

DBBC Setup and Operation



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IVS TOW, MIT-Haystack Observatory, May 2019

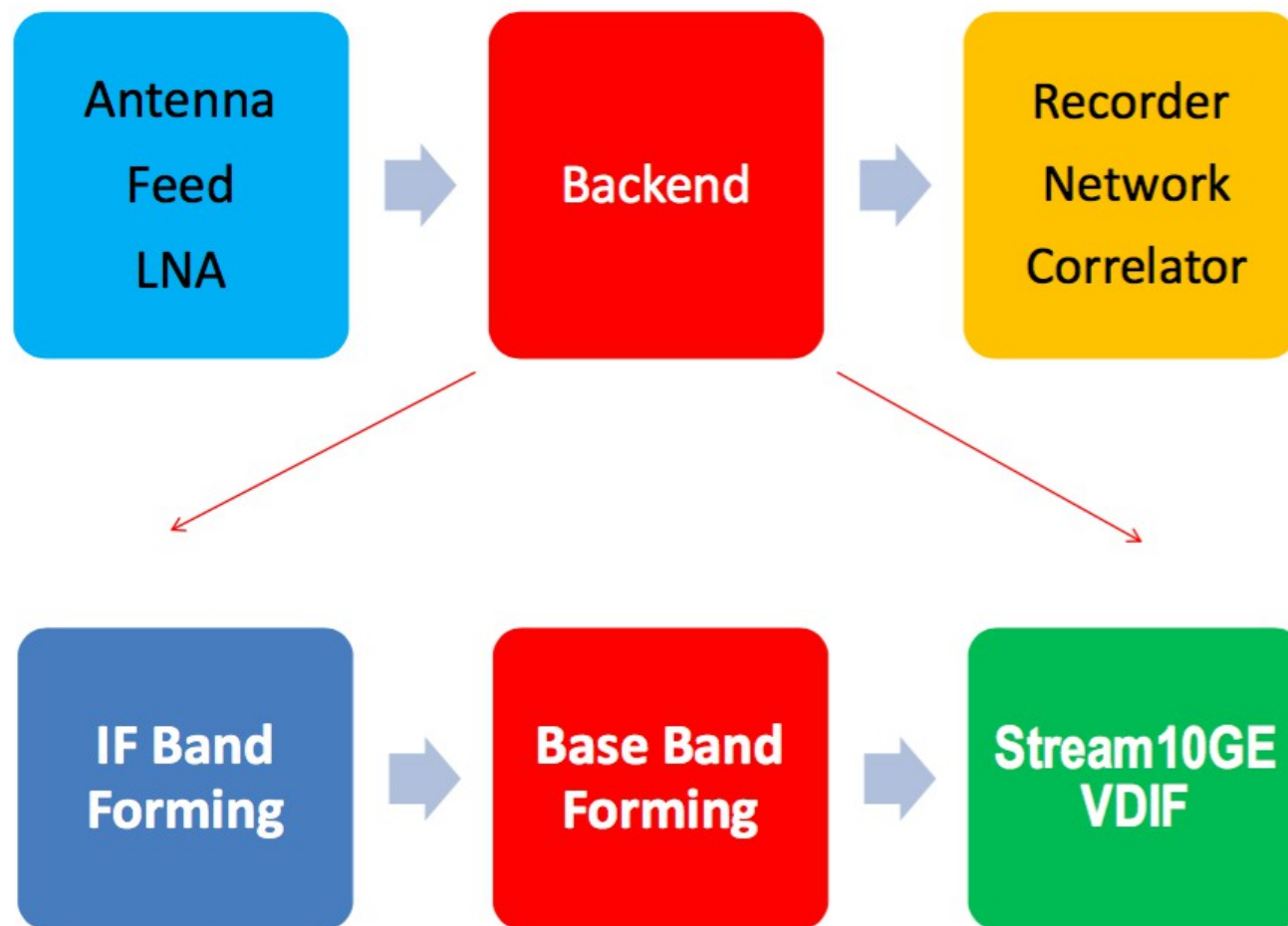


Content

- DBBC hardware characteristics
 - What is it good for
 - A tour around the DBBC
 - Component description
- Installation of a DBBC
- DBBC software
 - Poly-phase Filter Bank (PFB)
 - Digital Down Conversion (DDC)
- Basic testing
- Field System integration
- VLBI operation



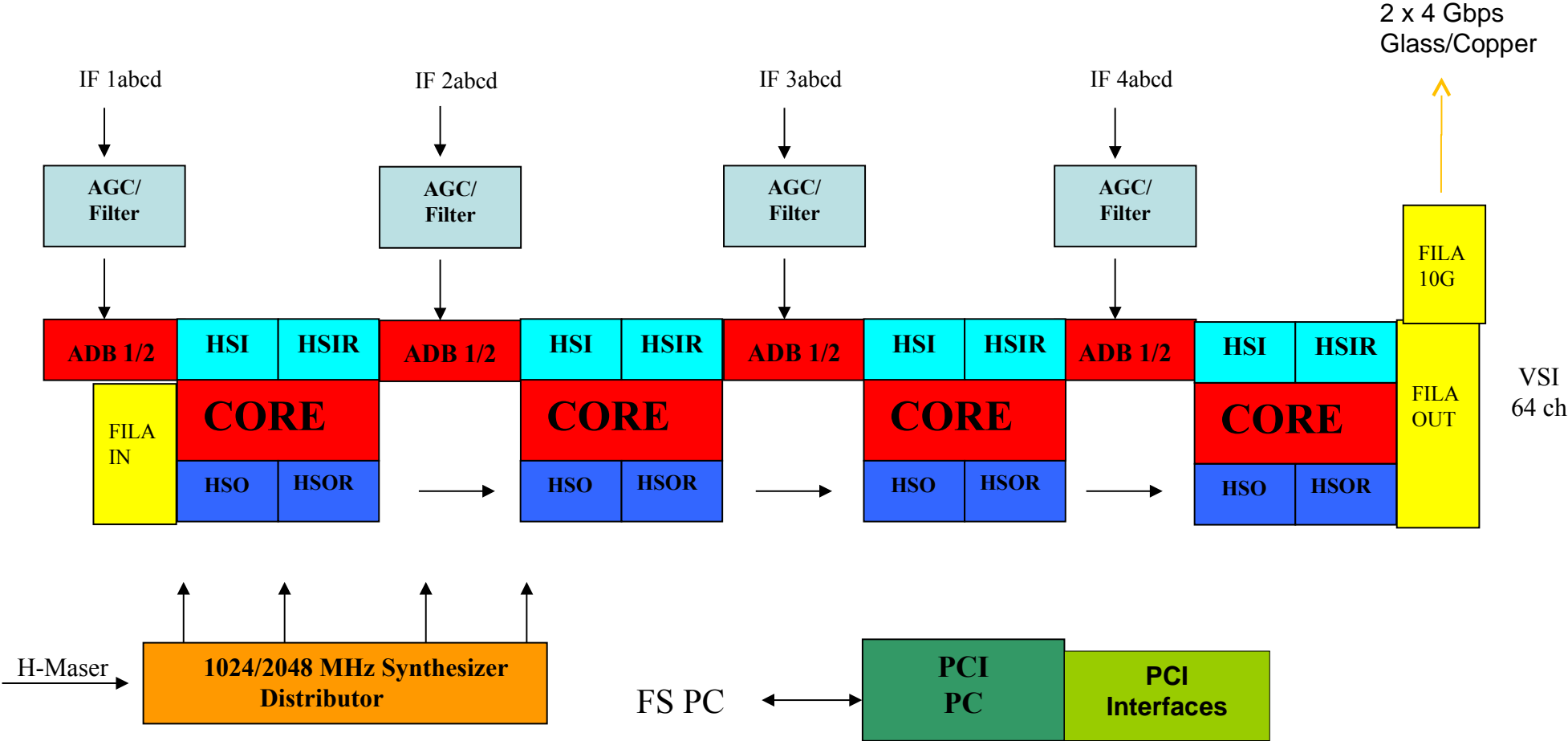
The VLBI backend





The DBBC Architecture

IF_n (MHz)
1~512, 512~1024, 1024~1536, 1536~2048
or
1~1024, 1024~2048 MHz

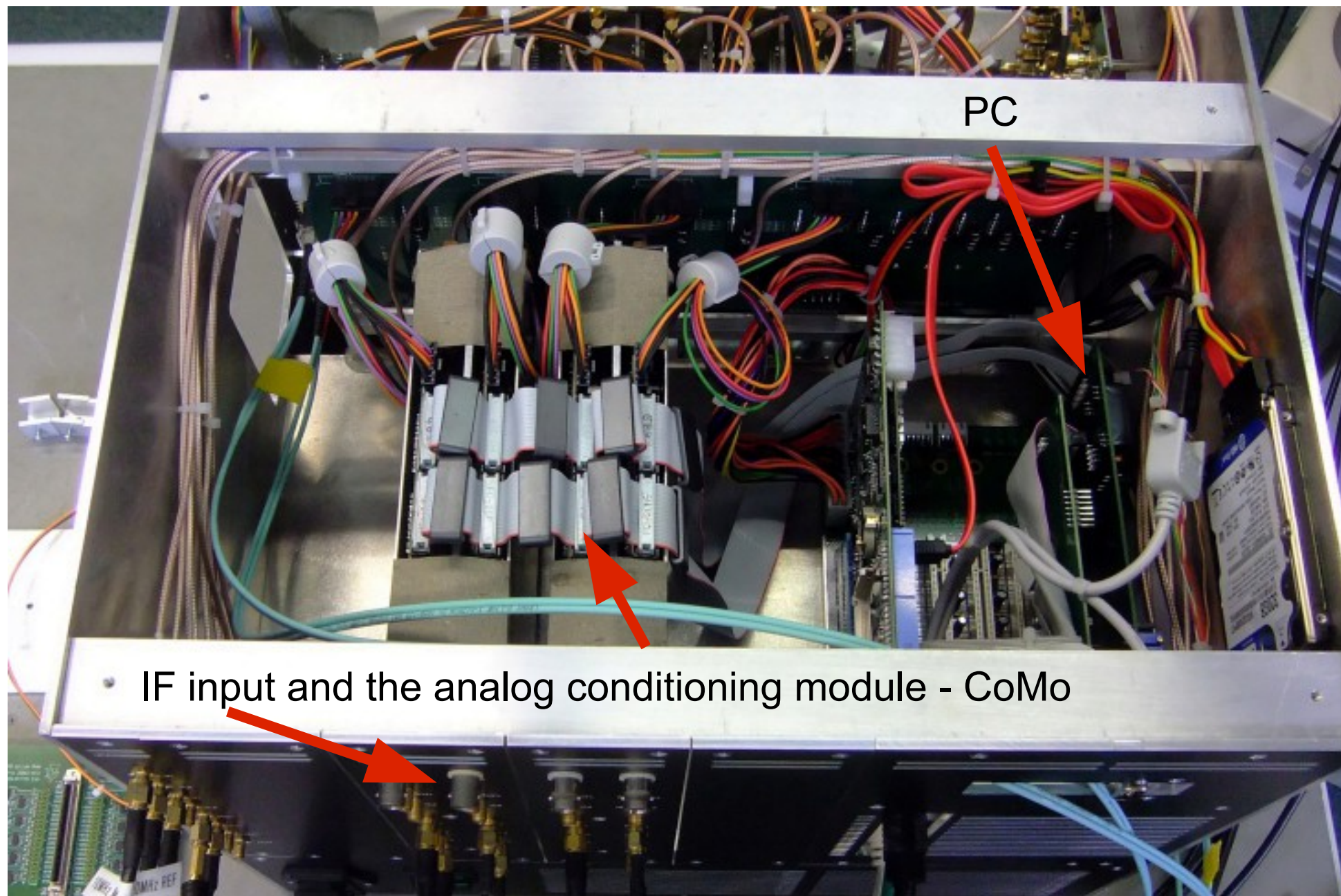


DBBC Outside (front view)

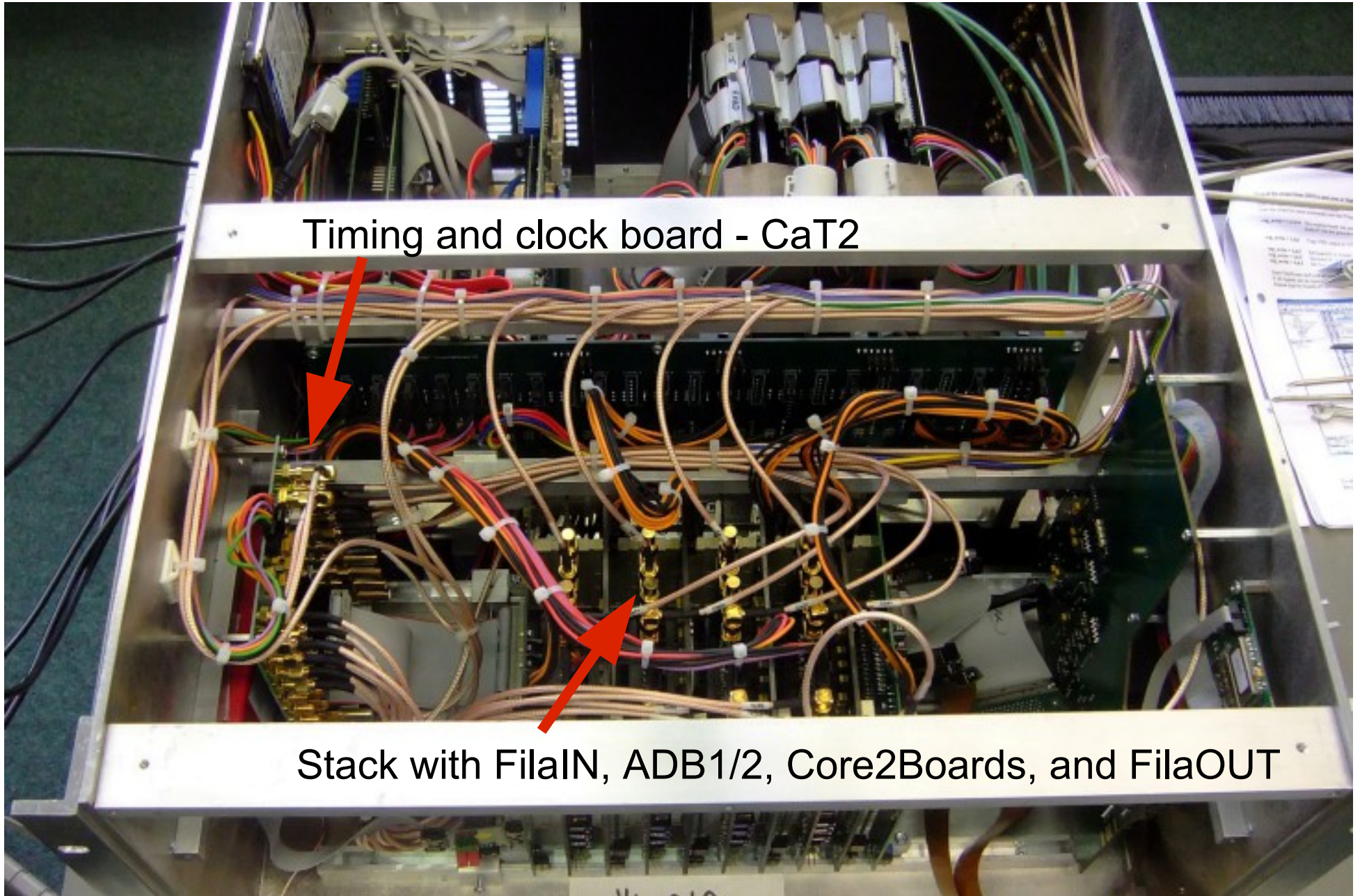




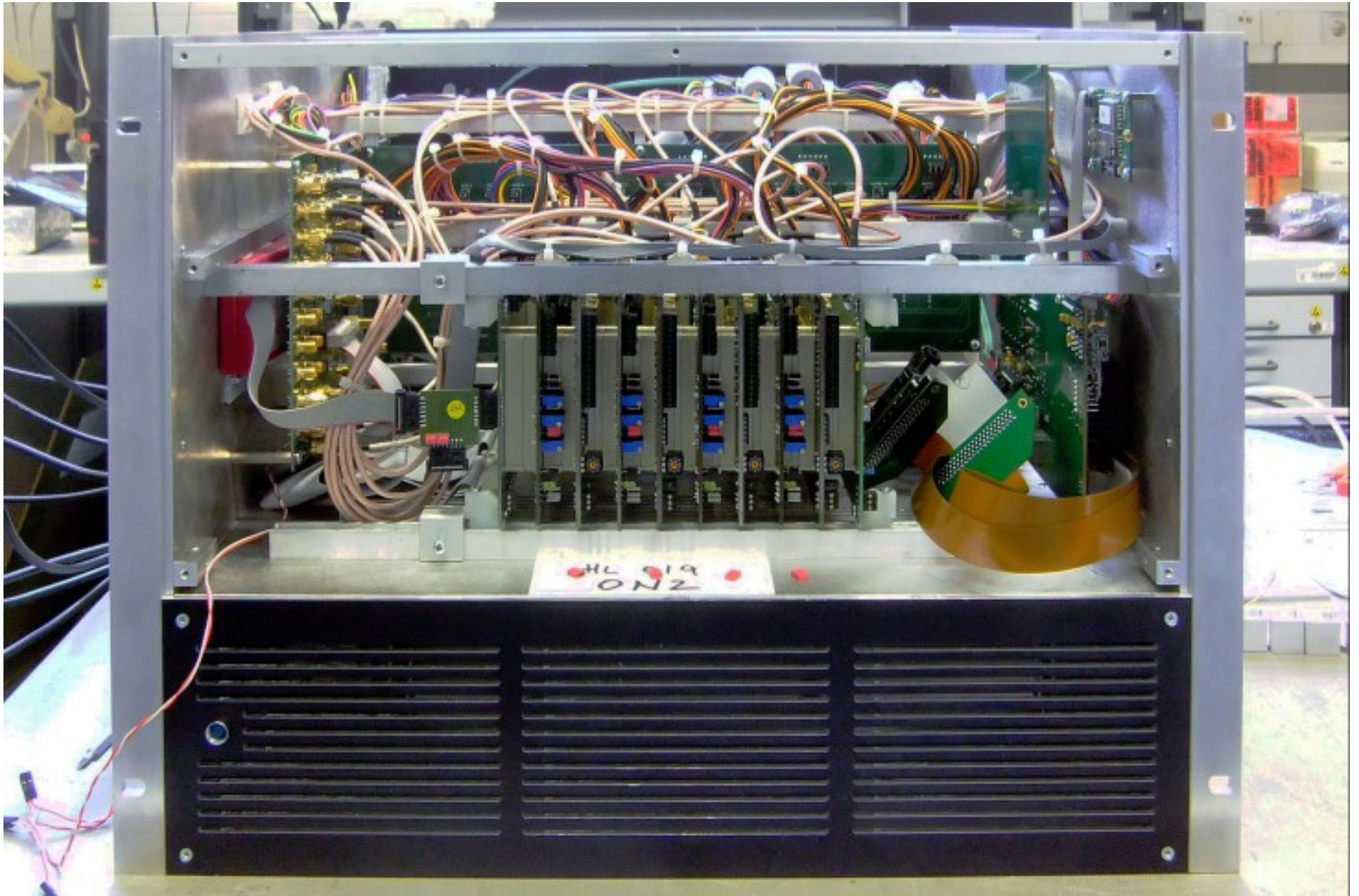
DBBC Inside



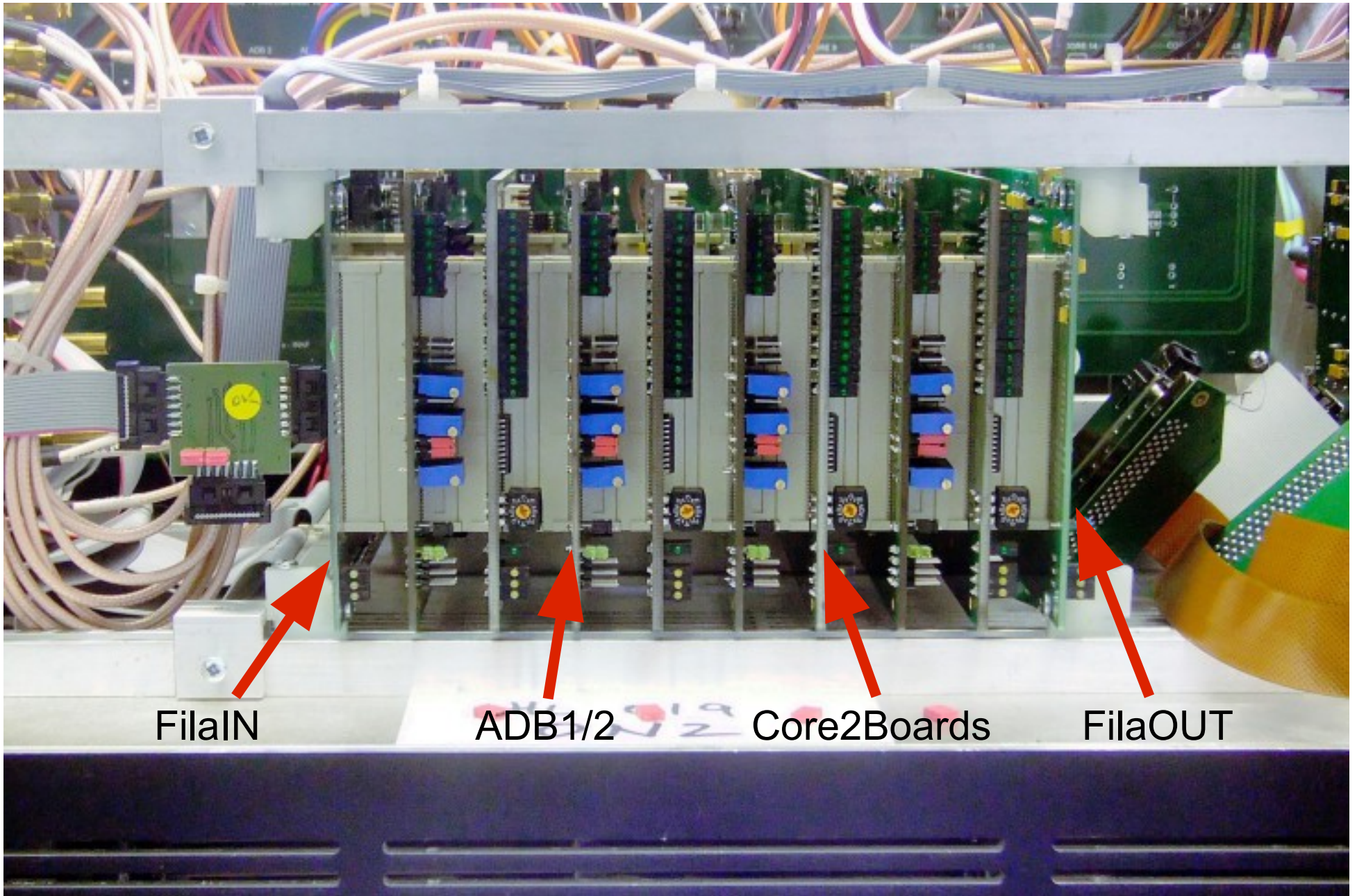
DBBC Inside



DBBC Inside



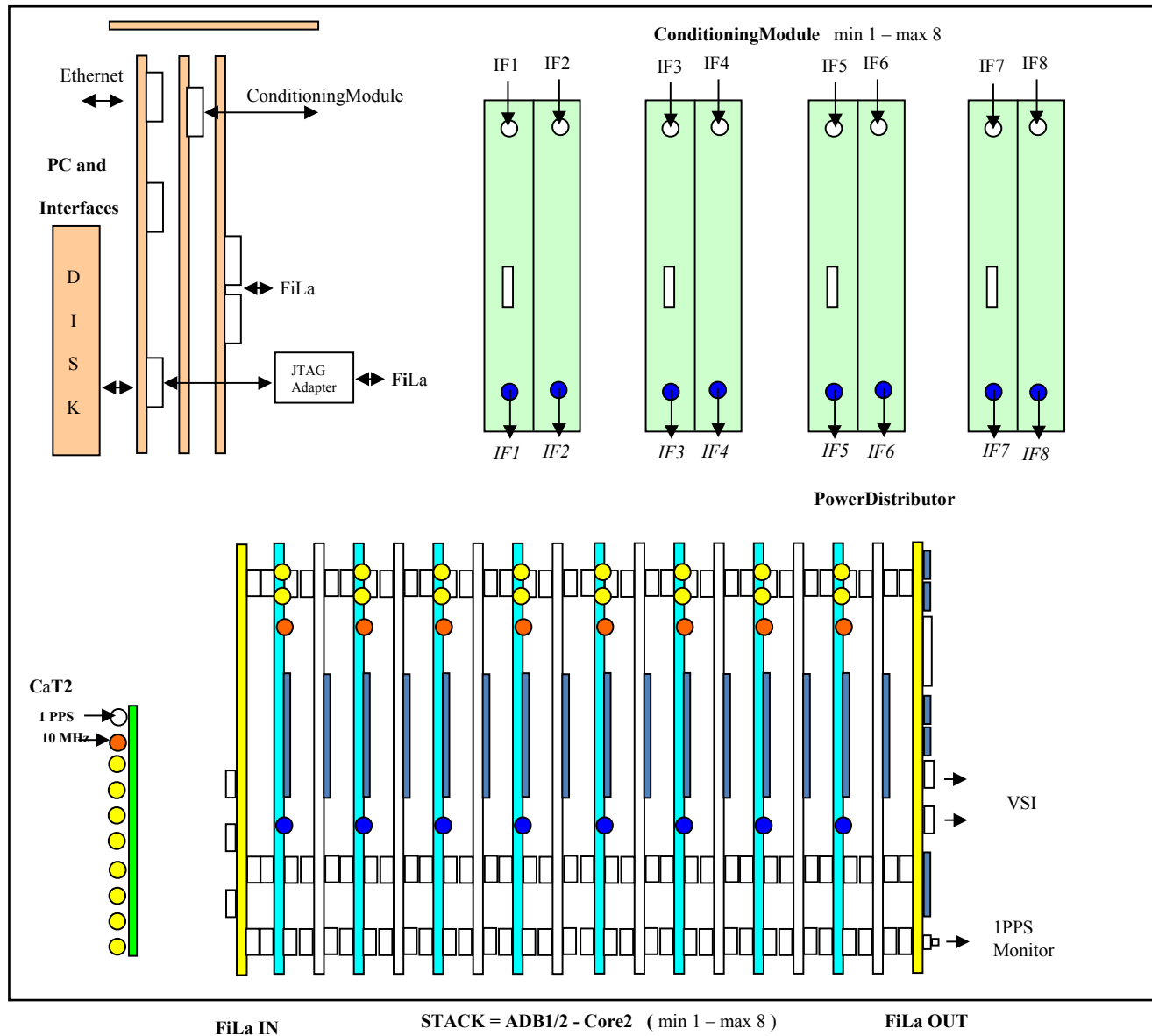
DBBC Inside





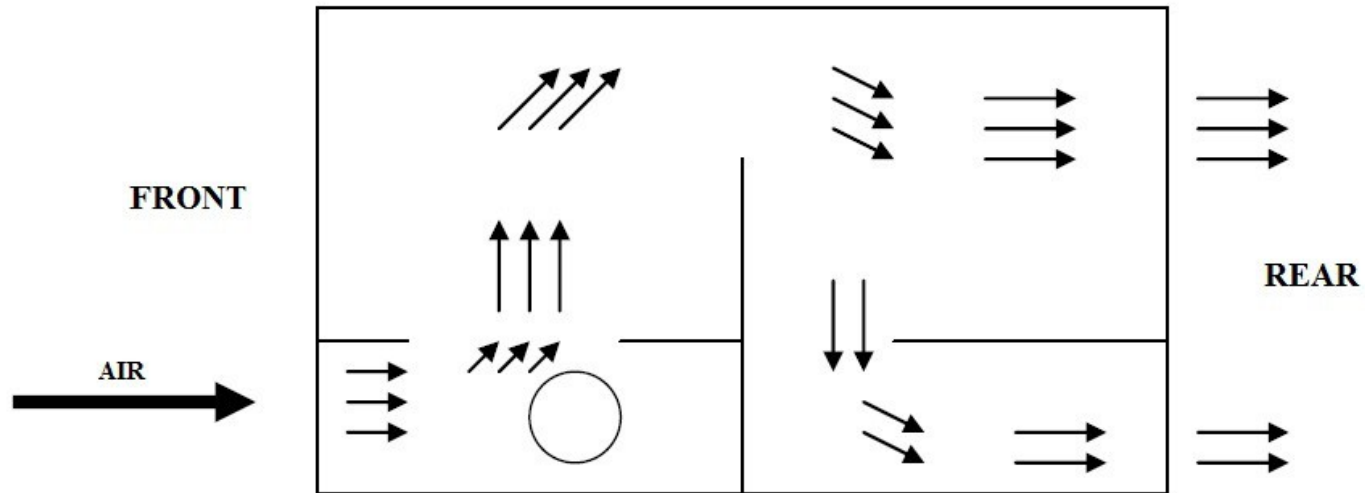
The DBBC Architecture

DBBC2 / DCCB2010 Schematic Top View





The DBBC Achitecture



The air cooling flow from a side view



General Features

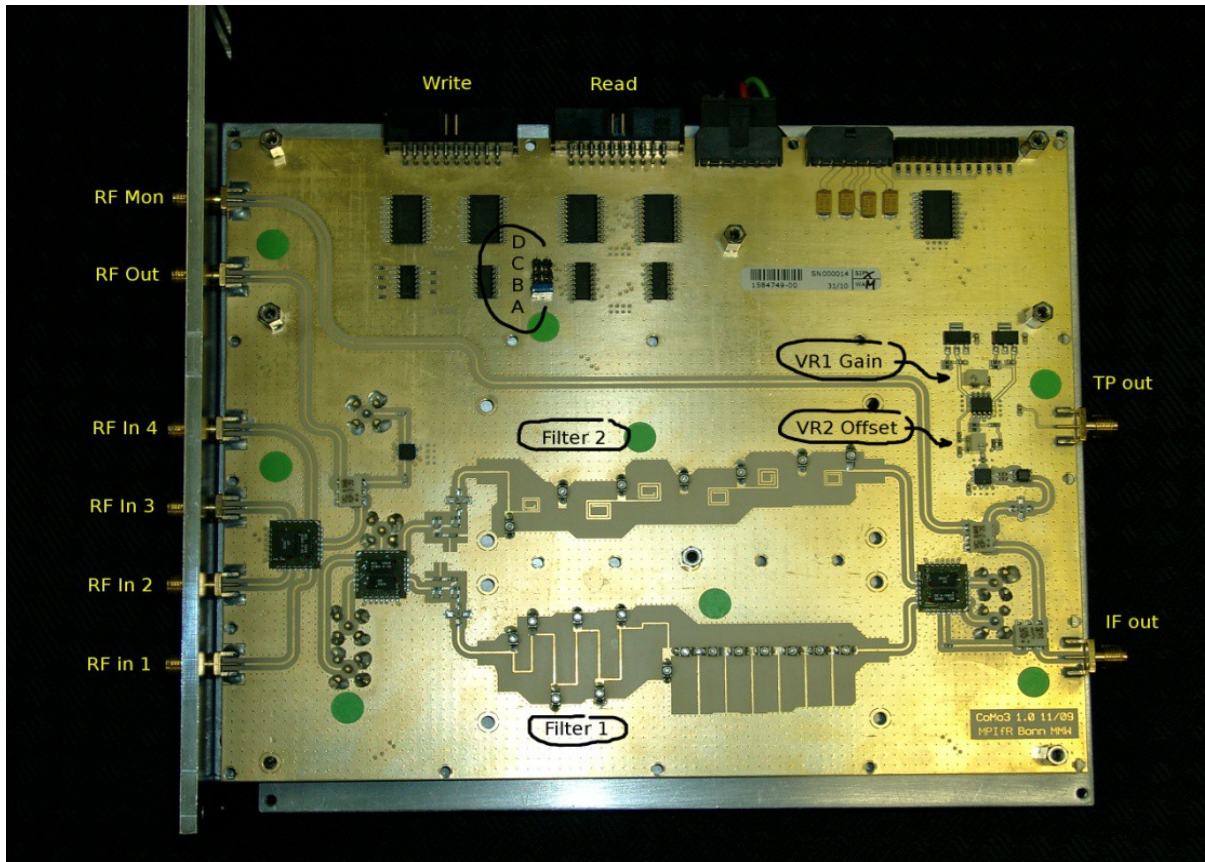
- 4/8 RF/IF Input out of 16 (4x4) in a range up to 2.2 (3.5) GHz
- 1024/2048 MHz sampling clock frequency
- Several personalities for different observing modes
- Input 4/8 polarizations / bands
- Output 4/8 groups of 32 data channel
- Output as VSI interfaces or as 10G Ethernet streams
- Control under Field System or other client console



Component description

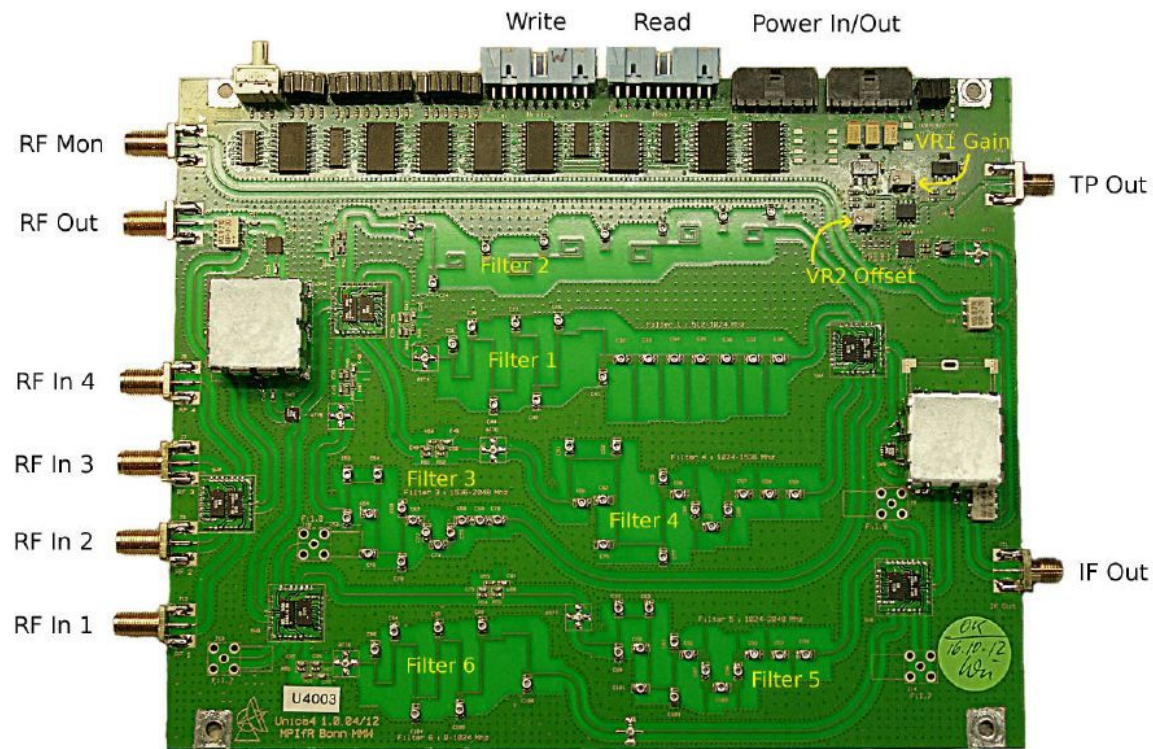
1. Analog Conditioning Module – CoMo
2. Analog-Digital Converter (ADB1 / ADB2)
3. Data Processing (Core2)
4. Connection and Service
(FiLaIN/OUT – FiLa10G FILA10G-4)
5. Timing and Clock (CaT2 – Clock and Timing)
6. Computer Control (PCSet)

1. Conditioning Module (Unica3)



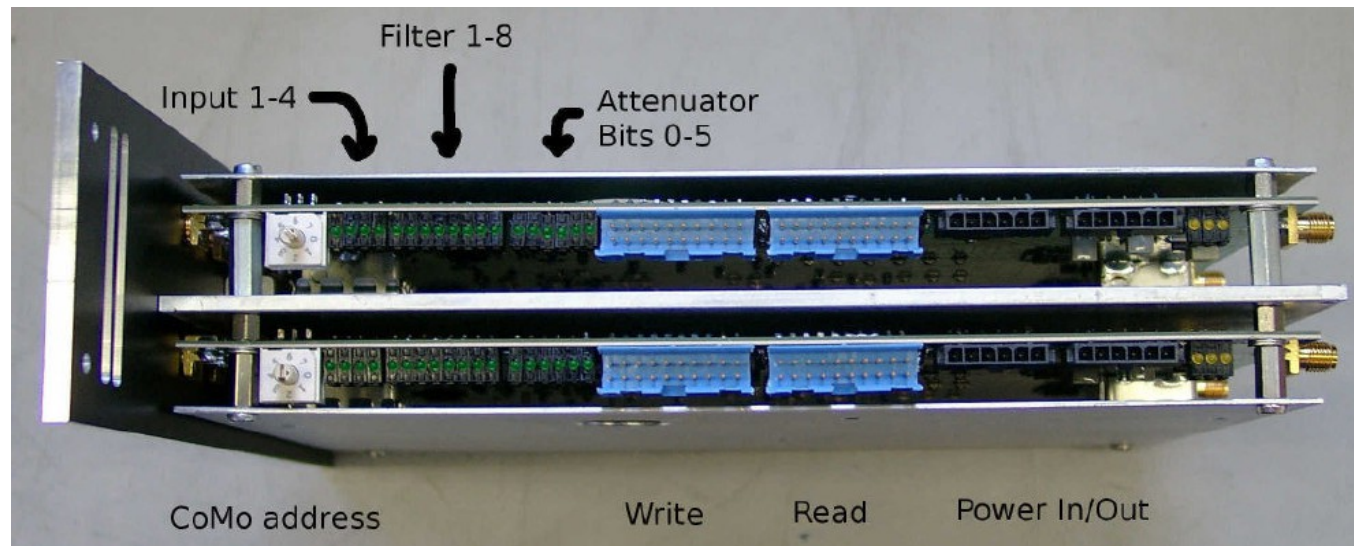
- 4 selectable RF inputs
- 4 selectable Nyquist filters
- 31.5 dB programmable attenuation
- Total power full band
- Manual or automatic gain control

1. Conditioning Module (Unica4)

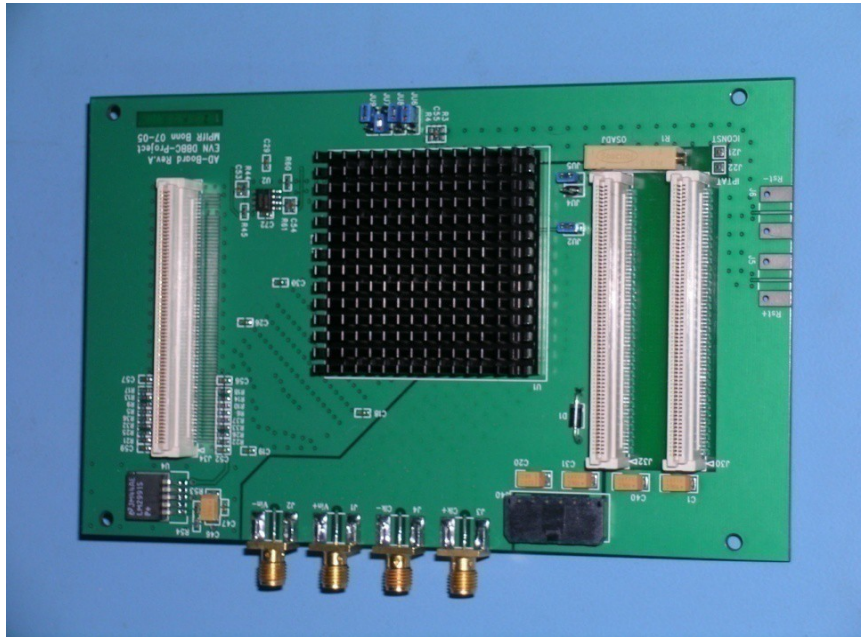


- Now with:
8 selectable Nyquist filters

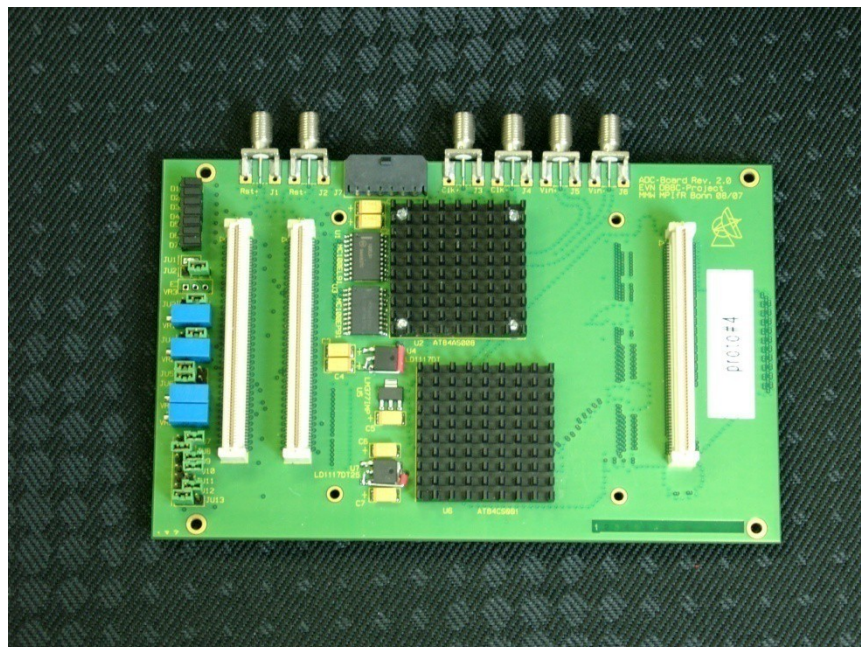
- 2 Unica boards build 1 CoMo



2. Analog to digital converter ADB1/2



- Analog input: 0 - 2.2 GHz
- Max Sampling clock 1.5 GHz
- Max Instantaneous bandwidth 750 MHz (real) / 1.5 GHz (complex)
- Output data 2 x 8-bit @ 1/4 Sclk DDR



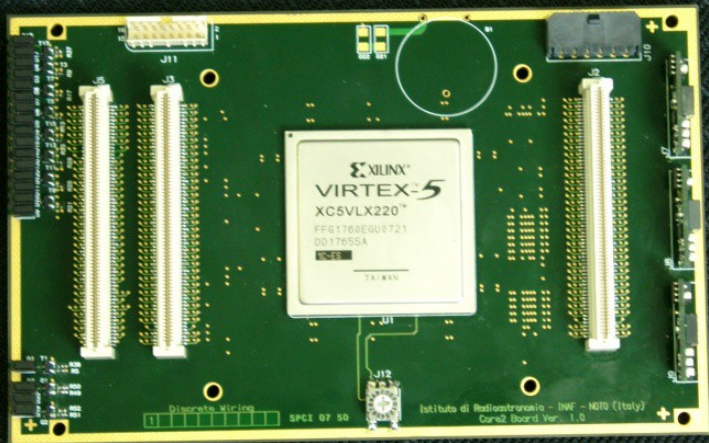
- Analog input: 0 – 3.5 GHz
- Max sampling clock 2.2 GHz
- Max instantaneous bandwidth 1.1 GHz (real) / 2.2 GHz (complex)
- Output data 2 x 8-bit @ 1/4 Sclk DDR
4 x 8-bit @ 1/8 Sclk DDR
- Piggy pack module support for 10-bit output and connection to Fila10G

3. Basic processing unit - Core2

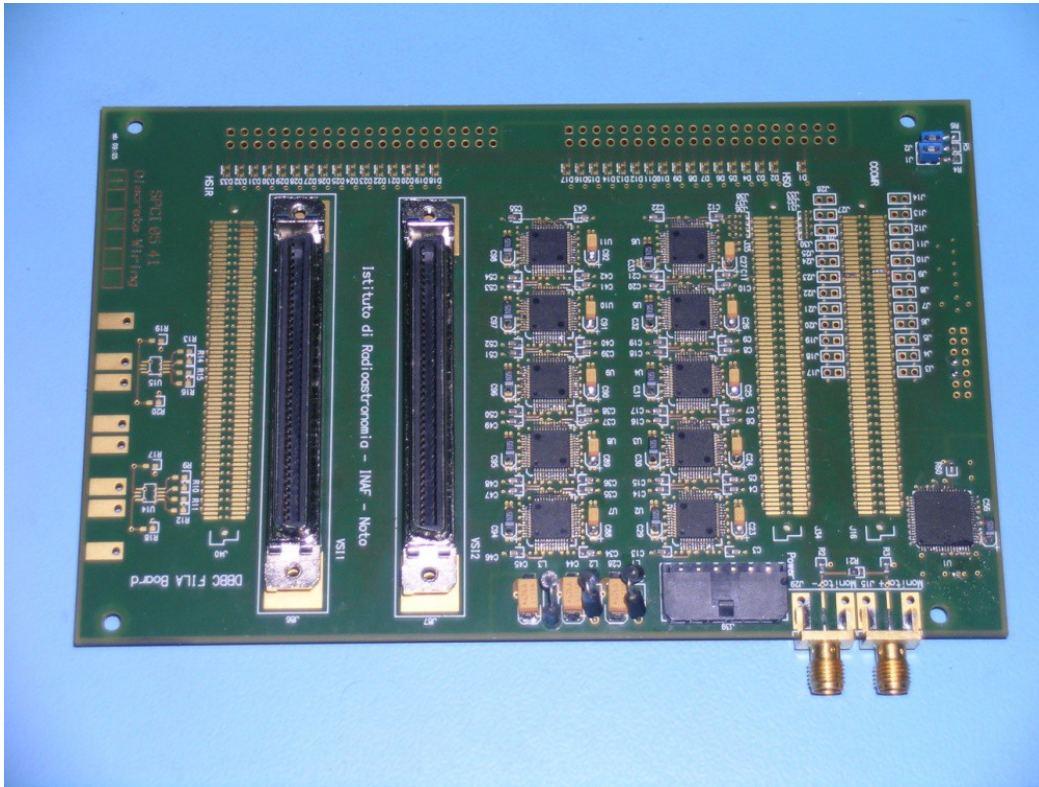
- Input rate:
(4 IF x 2 bus x 8-bit x SCIk/4 DDR) b/s
(2 IF x 4 bus x 8-bit x SCIk/8 DDR) b/s
.....

- Typical output rate:
(64 ch x 32-64-128) Mb/s
- Programmable architecture
 - Digital down conversion (DDC)
1 Core2 = 4 BBCs
 - Poly-phase Filter Bank (PFB)
1 Core2 = 16 Poly-phase filters

- 1 VSI 32 channel output



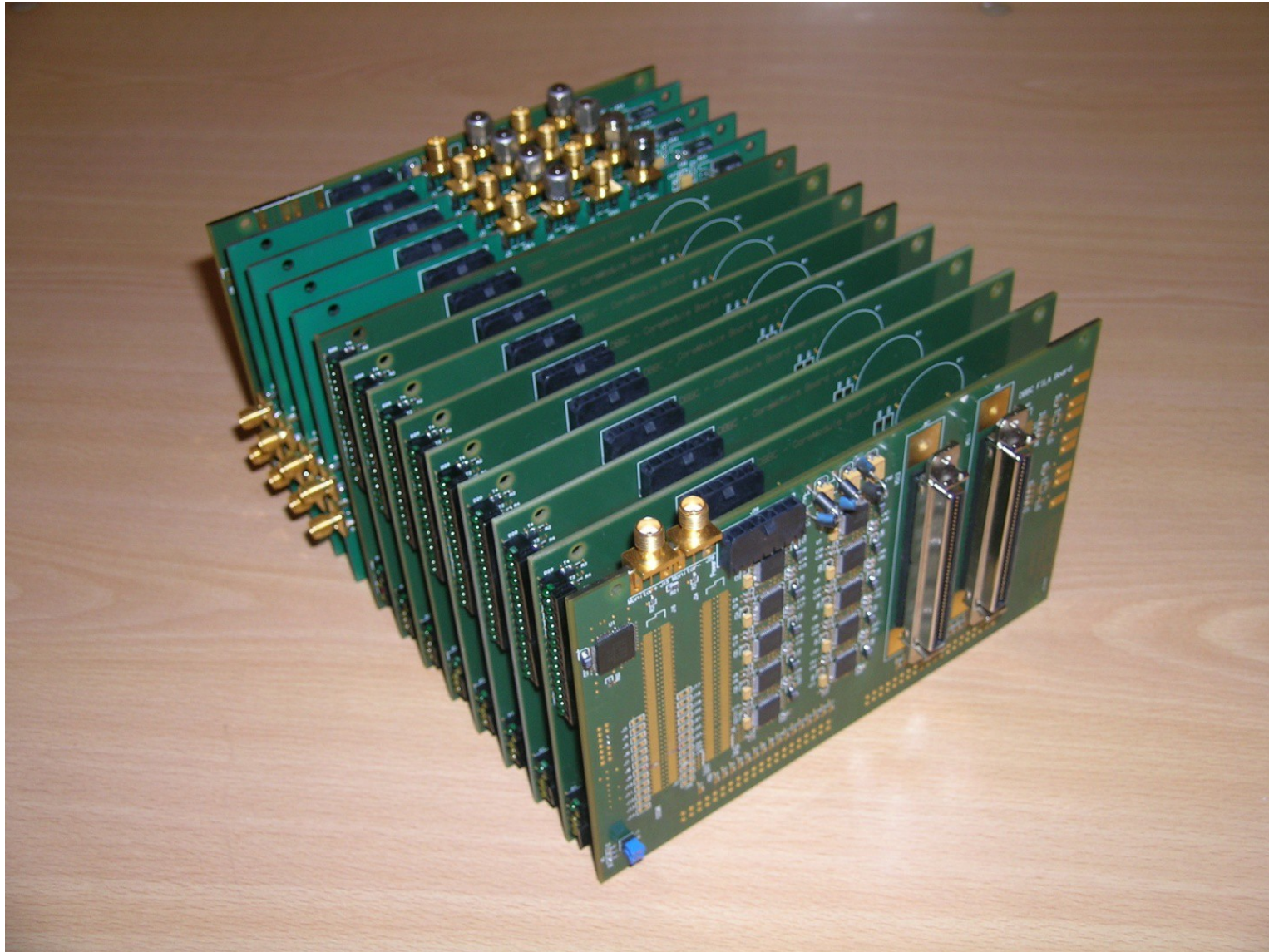
4. Connection and service - FiLaBoard



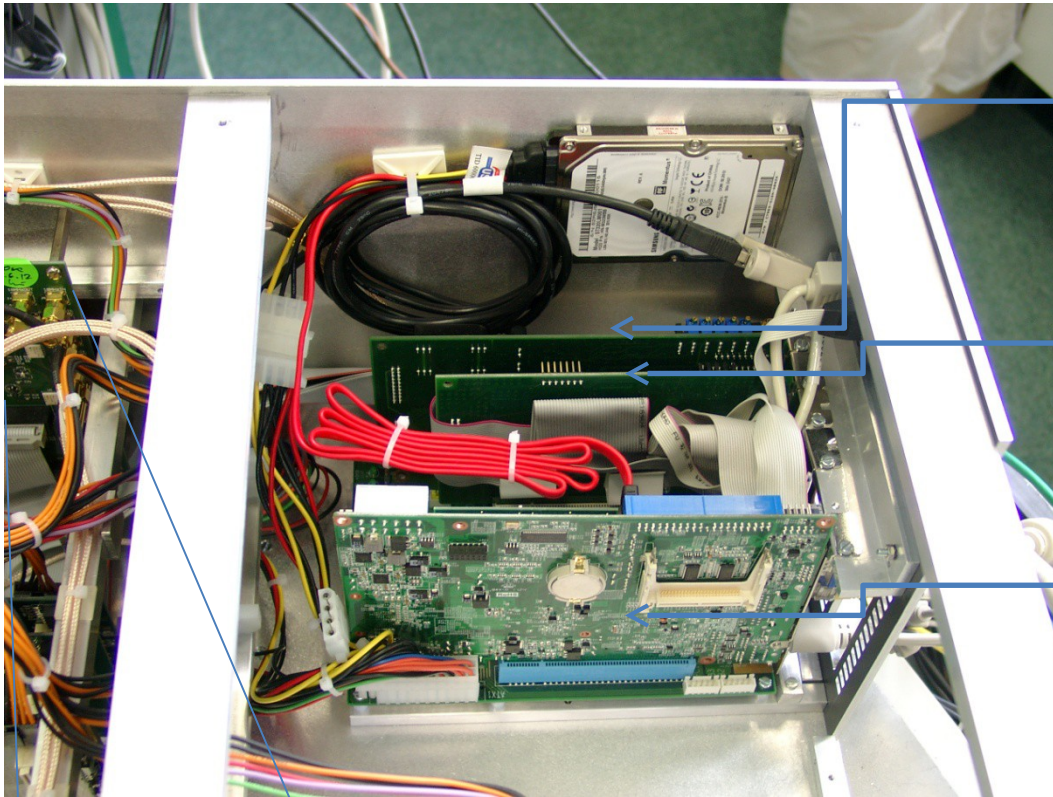
First and Last board in the stack

- First: IN
 - Communication interface
 - JTAG programming channel
 - 1pps in
- Last: OUT
 - 2 VSI interfaces
 - 1pps monitor out
 - 80 Hz continues calibration out

Complete Module Stack



6. PC Set – Control computer



ADLink PCI9111HR:
Communication with Conditioning Modules for IF total power measure, automatic gain control, registers control, etc.

ADLink PCI7200:
Communication with 32-bit bus for Core2 register setting, total power measurement, state statistics, etc.

Adventech PCI-7030:
Half Size PCI Motherboard (Intel Atom) on PCI backplane

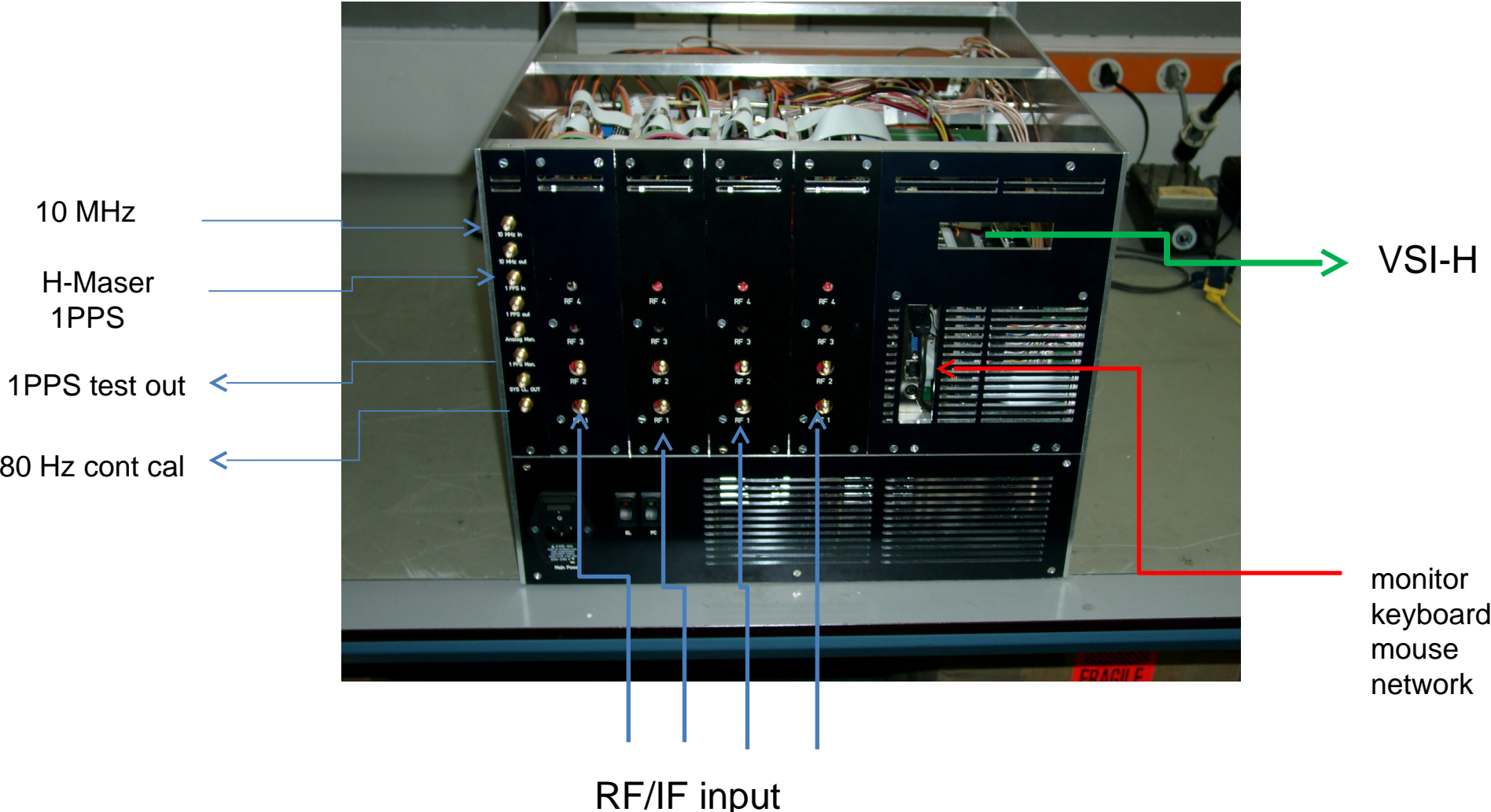
Xilinx programmer:
FPGA device configuration through USB – JTAG interface



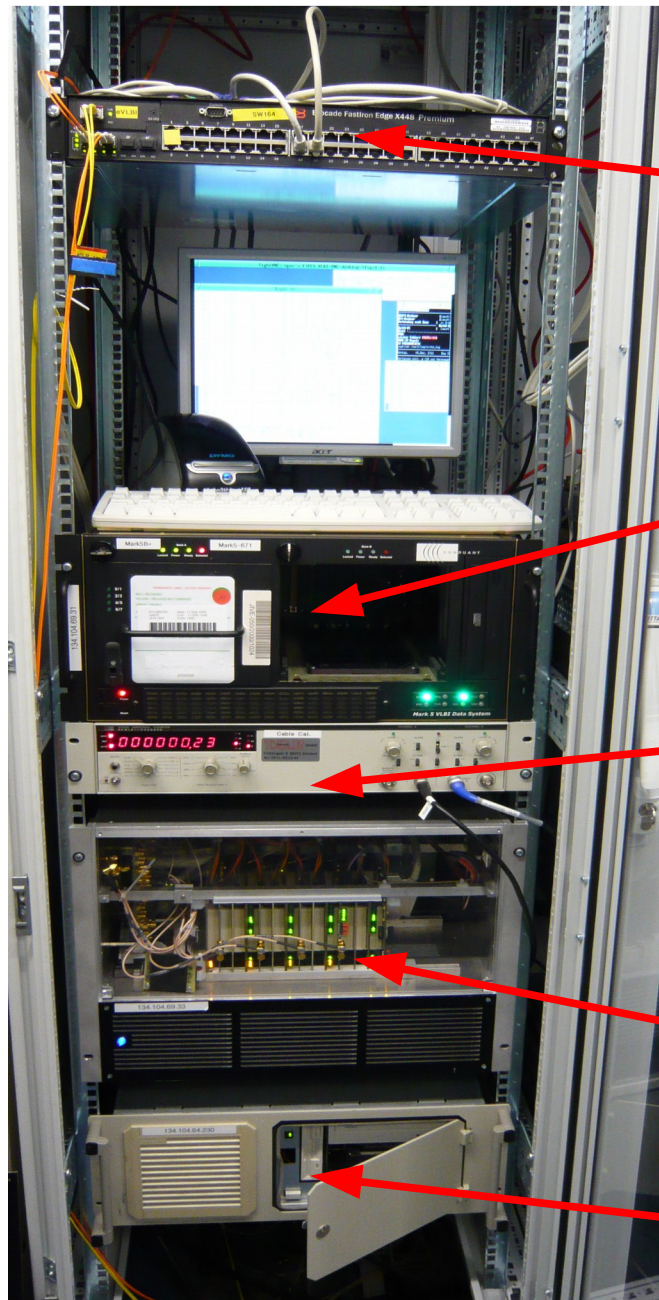


Installation of a DBBC

How to connect the DBBC



Installation of a DBBC



e-VLBI 10 GE switch

Mark5B+ disk recorder

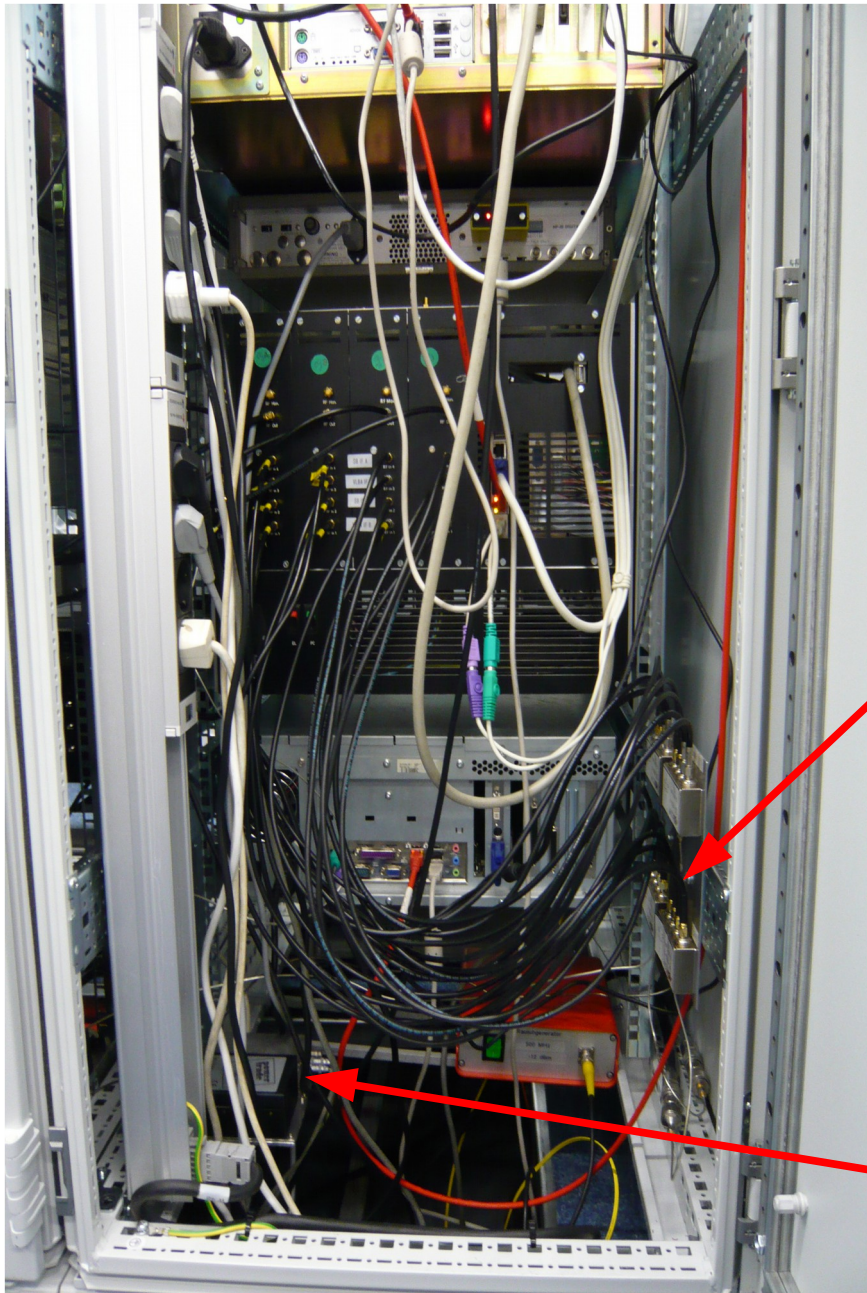
Counter to monitor
gps – 1pps out (MK5B)

DBBC

Field System PC



Installation of a DBBC

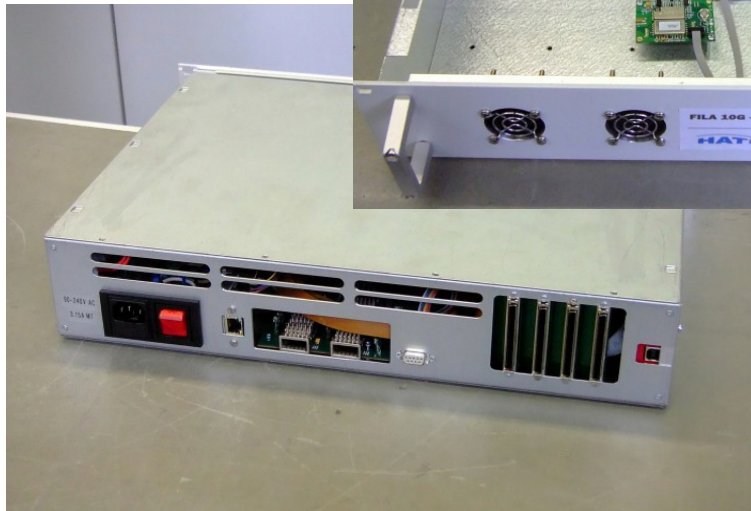
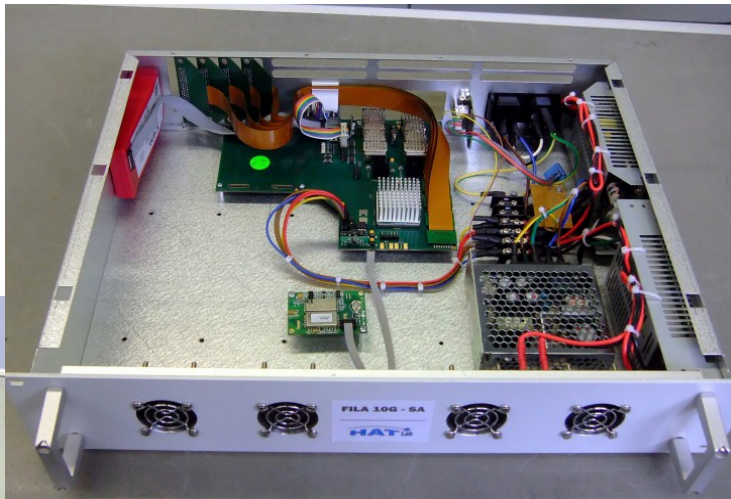
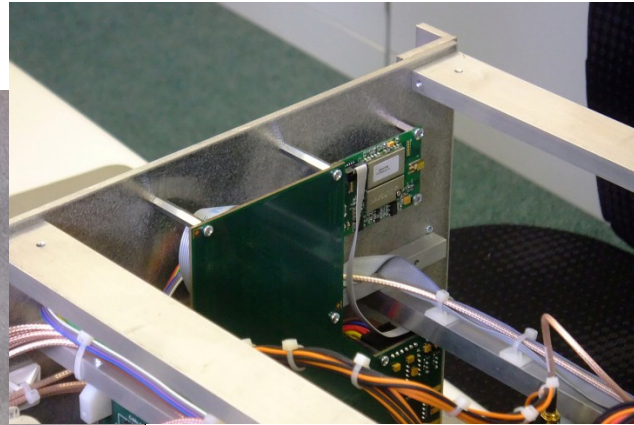
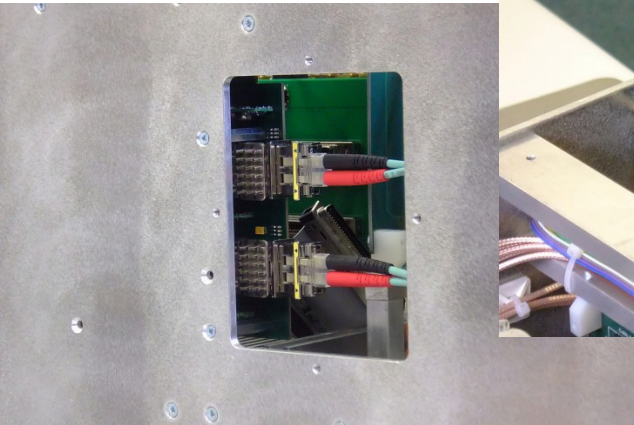


4x4 IF-Splitter to provide all possible IFs at the DBBC Inputs:

- IF1: a. 500-1000 IF RCP
b. 0-500 IF RCP
c. 500-1000 IF LCP
d. 0-500 IF LCP
- IF2: a. 500-1000 IF RCP
b. 0-500 IF RCP
c. 500-1000 IF LCP
d. 0-500 IF LCP
- IF3: a. 500-1000 IF RCP
b. 0-500 IF RCP
c. 500-1000 IF LCP
d. 0-500 IF LCP
- IF4: a. 500-1000 IF RCP
b. 0-500 IF RCP
c. 500-1000 IF LCP
d. 0-500 IF LCP

blank – sync generation from 80 Hz

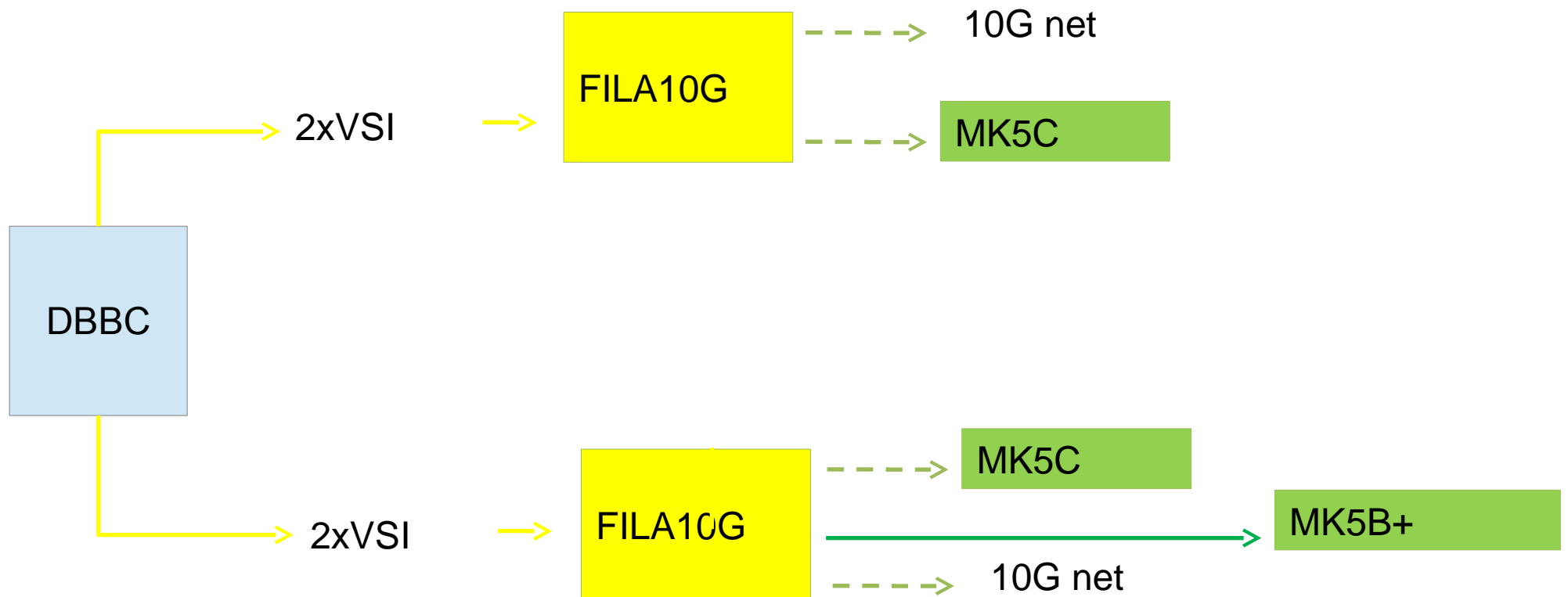
FiLa10G (SA)



- Two independent 10G Ethernet UDP port
- Physical interface optical XFP
- 10G port fully bidirectional
- Installed inside the DBBC box or as stand-alone
- Data rate: 1 – 2 – 4 Gbps each 10G port
- Format mode: RAW, MK5B or VDIF



Connection examples





FiLa10G Software

- **FILA10G Files:**

- c:\DBBC\bin\timesyncFILA10G.exe (MK5B time set)
 - c:\DBBC\bin\vdif_timesyncFILA10G.exe (VDIF time set)
 - c:\DBBC\bin\sendstr.exe (serial communication)
 - c:\DBBC_conf\FilesDBBC\fila10g_v3.3.1.bit
 - c:\DBBC\doc\DBBC2 FILA10G Command set v3.3.1.pdf

Note: a program to sync with a NTP server is required (eg. NetTimeSetup-314.exe) or new FiLa10G modules have a GPS module build in that can be used to get the GPS time.



Setting up the FiLa10G

- Upload of the firmware is
 - automatically made by the DDC/PFB control software (internal FiLa10G)
 - done with an additional Xilinx JTAG programmer using a script for IMAPCT (external FiLa10G-SA)
- Communication is through serial port or Ethernet in the stand-alone version
- Commands available (see document)
- VDIF packet size setting (see document)
- Script files can be used for block of commands (see batch)



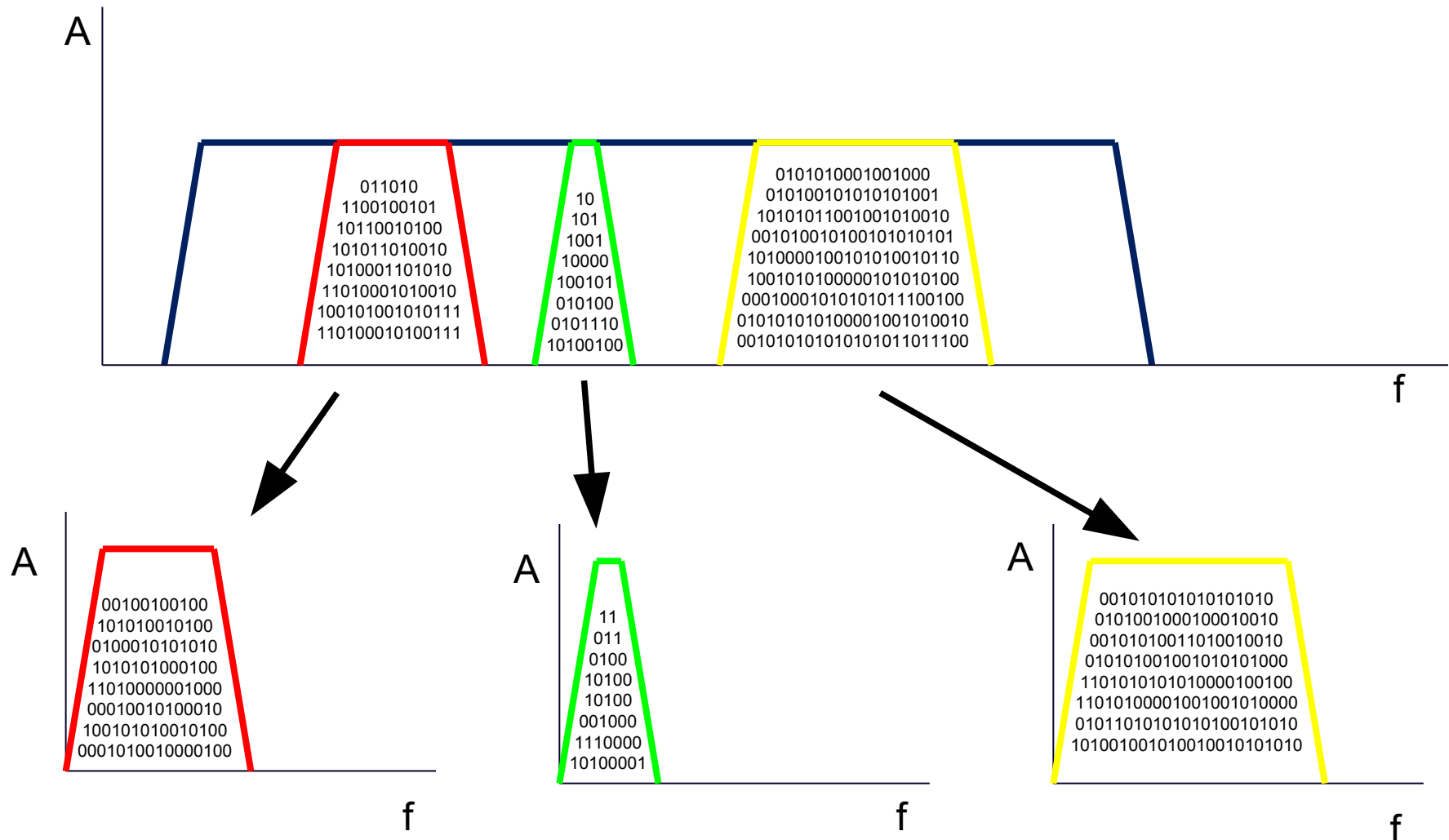
Observing modes

- DDC: tunable, channel bandwidth between 1 MHz and 64 MHz, U&L, Continuous cal with 80 Hz synchronization, modes: geo, astro, astro2, w-astro, lba, test
- PFB: fixed tuning, channel bandwidth 32/64 MHz, all U or L depending on the Nyquist zone
- DSC: full 4 x 512/1024 MHz, max 8 x 1024 MHz band direct sampling conversion, all U or L depending on the Nyquist zone
- SPECTRA: 4Kch/IF spectrometer, max 32K channels



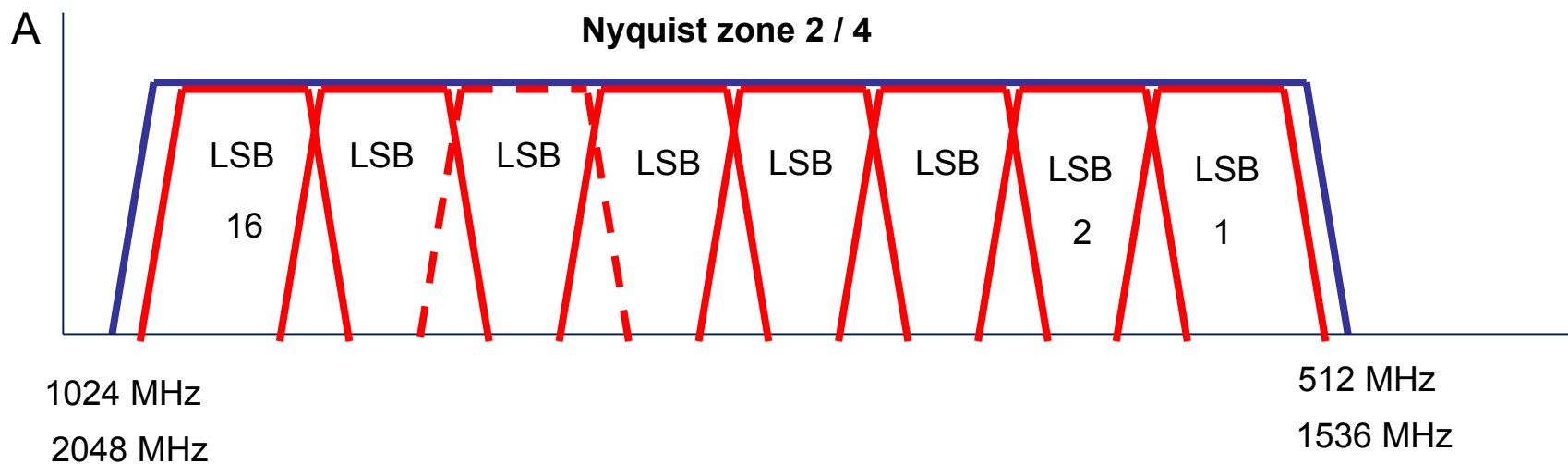
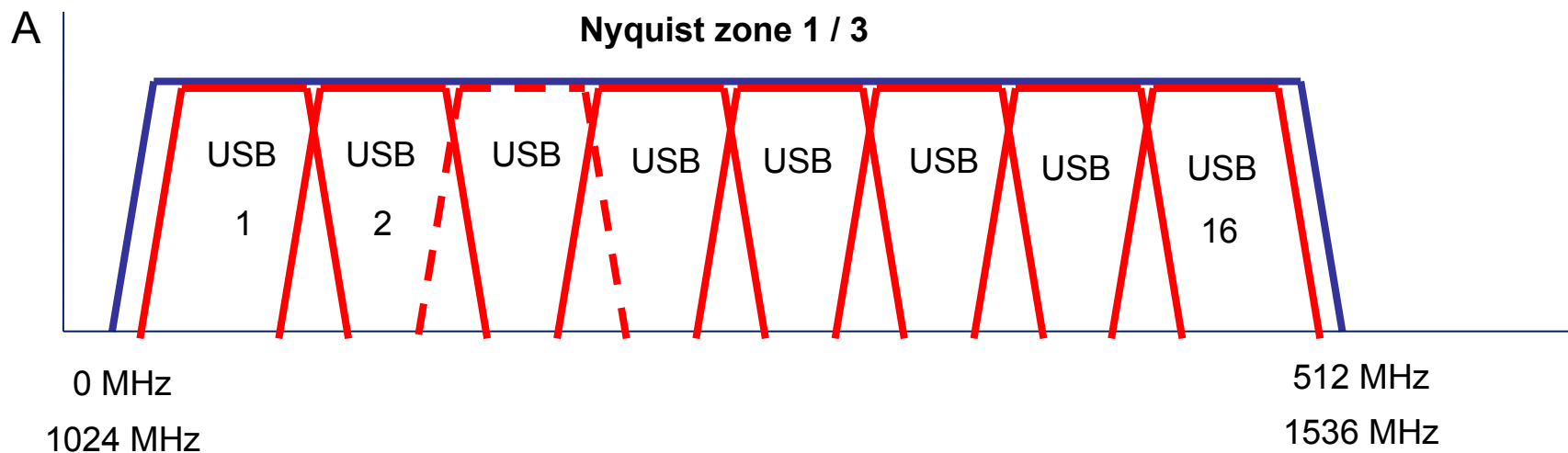
DDC – digital down conversion

Conversion to baseband, tunable channels of variable bandwidth





PFB – poly-phase filter bank





Software

How the observing mode is selected

- Using a dedicated firmware
- Using a dedicated control software
- Using a dedicated configuration text file



Software (Windows XP)

Files Structure:

C:\DBBC\bin
→ control software

C:\DBBC\doc
→ manuals

C:\DBBC_CONF\
→ configuration text files

C:\DBBC_CONF\FilesDBBC
→ firmware

rdesktop - 10.100.100.36

Normal DBBC Program DDC v104_2

```
Command from 134.104.64.233: Command received: dbbc05 6
Command from 134.104.64.233: Command received: dbbc06 6
Command from 134.104.64.233: Command received: dbbc07 6
Command from 134.104.64.233: Command received: dbbc08 6
Command from 134.104.64.233: Command received: dbbcifa 7
Command from 134.104.64.233: Command received: dbbcifb 7
Command from 134.104.64.233: Command received: dbbc01 6
Command from 134.104.64.233: Command received: dbbc02 6
Command from 134.104.64.233: Command received: dbbc03 6
Command from 134.104.64.233: Command received: dbbc04 6
Command from 134.104.64.233: Command received: dbbc05 6
Command from 134.104.64.233: Command received: dbbc06 6
Command from 134.104.64.233: Command received: dbbc07 6
Command from 134.104.64.233: Command received: dbbc08 6
Command from 134.104.64.233: Command received: dbbcifa 7
Command from 134.104.64.233: Command received: dbbcifb 7
Command from 134.104.64.233: Command received: dbbcifb 7
Command from 134.104.64.233: Command received: dbbcifb 7
Command from 134.104.64.233: Command received: dbbcifb 7
Command from 134.104.64.233: Command received: dbbcifb 7
Command from 134.104.64.233: Command received: dbbcifb 7
Command from 134.104.64.233: Connection lost.
Server restarted
Waiting for connection
```

Address C:\DBBC_CONF

Folders	Name	Size	Type	Date Modified
Local Disk (C:)	dbbc_config_file.txt	1 KB	Text Document	10/4/2012
ADLINK	dbbc_config_file_101.txt	1 KB	Text Document	7/11/2013
DBBC	dbbc_config_file_102.txt	1 KB	Text Document	11/19/2013
bin	dbbc_config_file_102b.txt	1 KB	Text Document	7/11/2013
manuals	dbbc_config_file_104.txt	1 KB	Text Document	12/11/2013
DBBC_CONF	dbbc_config_file_105.txt	1 KB	Text Document	3/19/2014
FilesDBBC	dbbc_config_file_105E.txt	1 KB	Text Document	4/23/2015
Documents and Settings	dbbc_config_file_105F.txt	1 KB	Text Document	3/19/2014
Intel	dbbc_config_file_120509.txt	1 KB	Text Document	10/17/2013

start Command Prompt Normal DBBC Progra... C:\DBBC_CONF 5:01 PM

<https://www.hat-lab.cloud>



Browser address bar: <https://www.hat-lab.cloud/downloads-dbbc2-ddc/>

Page title: Hat Lab






Navigation menu: HOME COMPANY PROFILE DBBC BACK-ENDS EVOLUTION ACTIVITY AND PLANS PRODUCTS FUNK HAUS DOWNLOAD LOGIN CONTACTS

Header: HAT Lab

Text: There are **5 files**, weighing **36.9 MiB** with **59 hits** in **DBBC2-DDC**.

Text: Displaying 1 to 5 of 5 files.

DBBC2-DDC

-  **DBBC2 DDC v105**
» **3.1 MiB - 6 hits - 20 April 2018**
DBBC2 DDC v105
-  **DBBC2_DDC_v106_261118.rar**
» **9.9 MiB - 5 hits - 26 November 2018**
DBBC2_DDC_v106_261118.rar
-  **DBBC2_DDC_v107_beta1.zip**
» **6.8 MiB - 16 hits - 20 November 2018**
DBBC2_DDC_v107_beta1.zip
-  **DBBC2_DDC_v107_beta2.rar**
» **8.4 MiB - 9 hits - 11 January 2019**
DBBC2_DDC_v107_beta2.rar
-  **DBBC2_DDC_v107_beta3.rar**
» **8.7 MiB - 23 hits - 30 January 2019**
DBBC2_DDC_v107_beta3.rar



Software

- DDC:

c:\DBBC\bin\DBBC2 Control DDC v107.exe (server)

c:\DBBC_conf\dbbc_config_file_107.txt

c:\DBBC_conf\FilesDBBC\dbbc2_ddc_v107.bit

c:\DBBC\doc\DBBC2 DDC command set v107.pdf

- PFB:

c:\DBBC\bin\DBBC2 Control PFB v16_2.exe (server)

c:\DBBC_conf\dbbc_poly_config_file_16.txt

c:\DBBC_conf\FilesDBBC\ dbbc2_pfb_v16.bit

c:\DBBC\doc\DBBC2 PFB command set v16.pdf



DDC configuration file

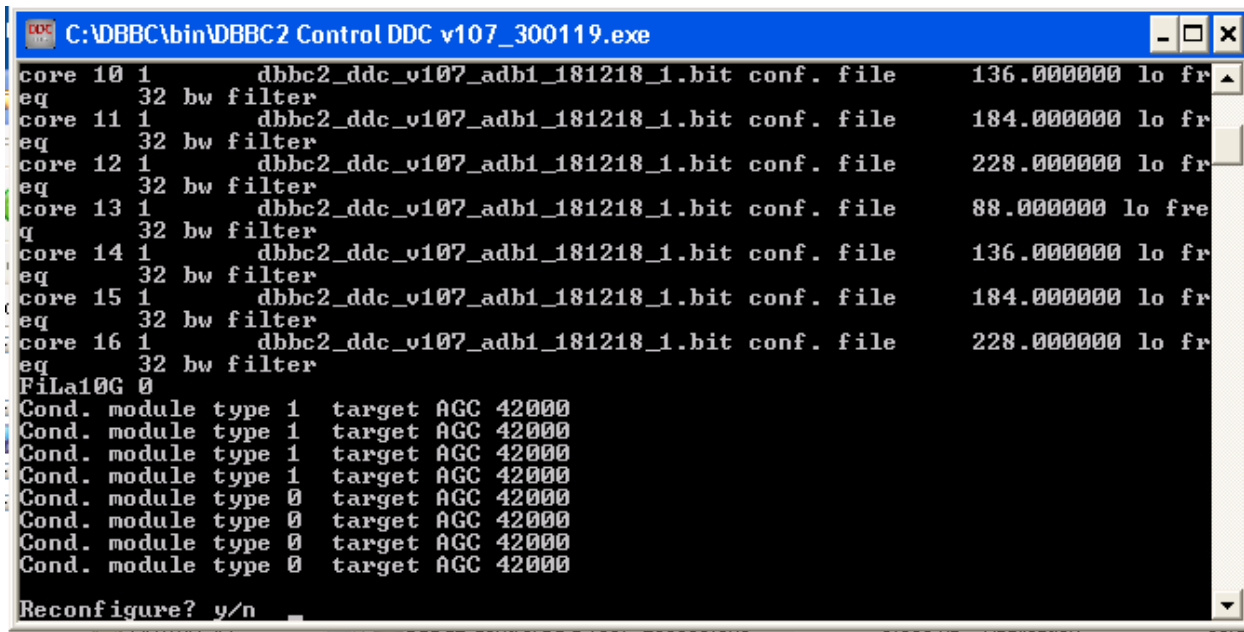
c:\DBBC_conf\dbbc_config_file_v107.txt

Example:

```
1 dbbc2_ddc_v107.bit 597.00 8 ← the first number is indication of ADB1|2, in this case ADB1 is on
1 dbbc2_ddc_v107.bit 682.00 8 IFA and ADB2 on IFB, ADB1 in IFC, no Core2 for IFD
1 dbbc2_ddc_v107.bit 853.00 8 If no Core2 is inserted in the first and second column put 0.
1 dbbc2_ddc_v107.bit 938.00 8 The second parameter is the firmware file name to be used.
2 dbbc2_ddc_v107.bit 597.00 8 The third and fourth parameters are frequency and bandwidth respectively.
2 dbbc2_ddc_v107.bit 682.00 8
2 dbbc2_ddc_v107.bit 853.00 8
2 dbbc2_ddc_v107.bit 938.00 8
1 dbbc2_ddc_v107.bit 597.00 8
1 dbbc2_ddc_v107.bit 682.00 8
1 dbbc2_ddc_v107.bit 853.00 8
1 dbbc2_ddc_v107.bit 938.00 8
0 dbbc2_ddc_v107.bit 597.00 8 Each Core2 board supports 4 bbcs so if not present 0 has to be inserted in
0 dbbc2_ddc_v107.bit 682.00 8 four lines
0 dbbc2_ddc_v107.bit 853.00 8
0 dbbc2_ddc_v107.bit 938.00 8
1 fla10g_v2_1.bit COM2 ← if installed set 1st version 1 (with ACE), 2nd version (without ACE 2), otherwise 0, ser. port
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFA
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFB
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFC
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFD
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFE
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFF
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFG
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFH
107 112 0 0 ← phase calibration values
CAT2 1024 ← CAT1|2 and sampling frequency
PROG 0 3 ← jtag programmer: 0=xilinx, 1=digilent; prog freq. 3/6 MHz
```

Starting the software

DDC: running **DBBC2 Control DDC v107.exe**



```
C:\DBBC\bin\DBBC2 Control DDC v107_300119.exe
core 10 1 dbbc2_ddc_v107_adb1_181218_1.bit conf. file 136.000000 lo fr
eq 32 bw filter
core 11 1 dbbc2_ddc_v107_adb1_181218_1.bit conf. file 184.000000 lo fr
eq 32 bw filter
core 12 1 dbbc2_ddc_v107_adb1_181218_1.bit conf. file 228.000000 lo fr
eq 32 bw filter
core 13 1 dbbc2_ddc_v107_adb1_181218_1.bit conf. file 88.000000 lo fre
q 32 bw filter
core 14 1 dbbc2_ddc_v107_adb1_181218_1.bit conf. file 136.000000 lo fr
eq 32 bw filter
core 15 1 dbbc2_ddc_v107_adb1_181218_1.bit conf. file 184.000000 lo fr
eq 32 bw filter
core 16 1 dbbc2_ddc_v107_adb1_181218_1.bit conf. file 228.000000 lo fr
eq 32 bw filter
Fila10G 0
Cond. module type 1 target AGC 42000
Cond. module type 1 target AGC 42000
Cond. module type 1 target AGC 42000
Cond. module type 1 target AGC 42000
Cond. module type 0 target AGC 42000
Cond. module type 0 target AGC 42000
Cond. module type 0 target AGC 42000
Cond. module type 0 target AGC 42000
Reconfigure? y/n
```

after the Core2 configuration is completed

then run a client ex. **DBBC Client v3.exe** or **Field System**

DDC Mode Commands and Form Table (see documents)



First tests with the DBBC

- Cabling the DBBC: IF, 1pps, 10 MHz, (80 Hz calibration?)
- Starting the DDC software (server) on the DBBC Windows PC
 - Newest version always available at <http://www.hat-lab.cloud> currently v105/v106 or v107 beta3 for DDC
- Configuration file needs to be edit for your hardware installation.

First functionality can be tested with the DBBC_client or from the FS:

- select different IF inputs for the ADBs and let AGC adjustment work, e.g.

```
> dbbcifa # for query
```

```
> dbbcifa=2,agc,2 # to set RF input 2, agc on, IF filter 2 (0-500 MHz)
```

read out BBCs set different frequencies, ...

```
> dbbc01 # for query
```

```
> dbbc01=596.00,a,16.00 # to set BBC freq=596 MHz, IFA, BBC  
band width = 16 MHz
```




First tests with the DBBC

- > dbbcifa # for query
- > dbbcifa=2,agc,2 # to set RF input 2, agc on, IF filter 2 (0-500 MHz)

read out BBCs set different frequencies, ...

- > dbbc01 # for query
- > dbbc01=596.00,a,16.00 # to set BBC freq=596 MHz, IFA, BBC band width = 16 MHz

```
DBBC client v3.exe
Enter Command: dbbcifa
Received from DBBC: dbbcifa/2,0,agc,2,0,38000

Enter Command: dbbcifa
Received from DBBC: dbbcifa/2,0,agc,2,0,38000

Enter Command: dbbcifb
Received from DBBC: dbbcifb/3,0,agc,1,0,38000

Enter Command: dbbcifc
Received from DBBC: dbbcifc/4,0,agc,2,0,38000

Enter Command: dbbc01
Received from DBBC: dbbc01/124.490000,a,8,1,agc,255,255,4639,4486,4644,4492

Enter Command: dbbc02
Received from DBBC: dbbc02/140.490000,a,8,1,agc,255,255,5140,4758,5117,4745

Enter Command: dbbcifb=2,agc,2
Received from DBBC: dbbcifb/2,0,agc,2,0,38000

Enter Command: dbbcifb
Received from DBBC: dbbcifb/2,0,agc,2,0,38000

Enter Command:
```



Connecting a Mark5B(+)

Connect the DBBC VSI1 port to the Mark5B using VSI cable.

Set Mark5B needs to be synced to the 1pps on the VSI cable.

```
tstDIM > clock_set=32:ext
```

```
tstDIM > 1pps_source=vsi
```

```
tstDIM > dot_set=:force
```

```
tstDIM > dot?           # query several times to see if it stays synced
```

Test the quality of the connection

```
DBBC > dbbcform=test,tvg           # starts TVG on the DBBC
```

```
tstDIM > tvr=0xffffffff           # TVR LED should be green.
```

If it is not green it might help to carefully disconnect and reconnect the VSI cable on both ends, sometimes cleaning the connectors with dry air is required.

For testing with a Flexbuff or Mark6 it is recommended to use the FS



Calibration of the DBBC

Calibration or phase optimization is required at the system installation and has to be repeated after a hardware modification in the stack, transportation, or a new firmware. Periodically as a general check.

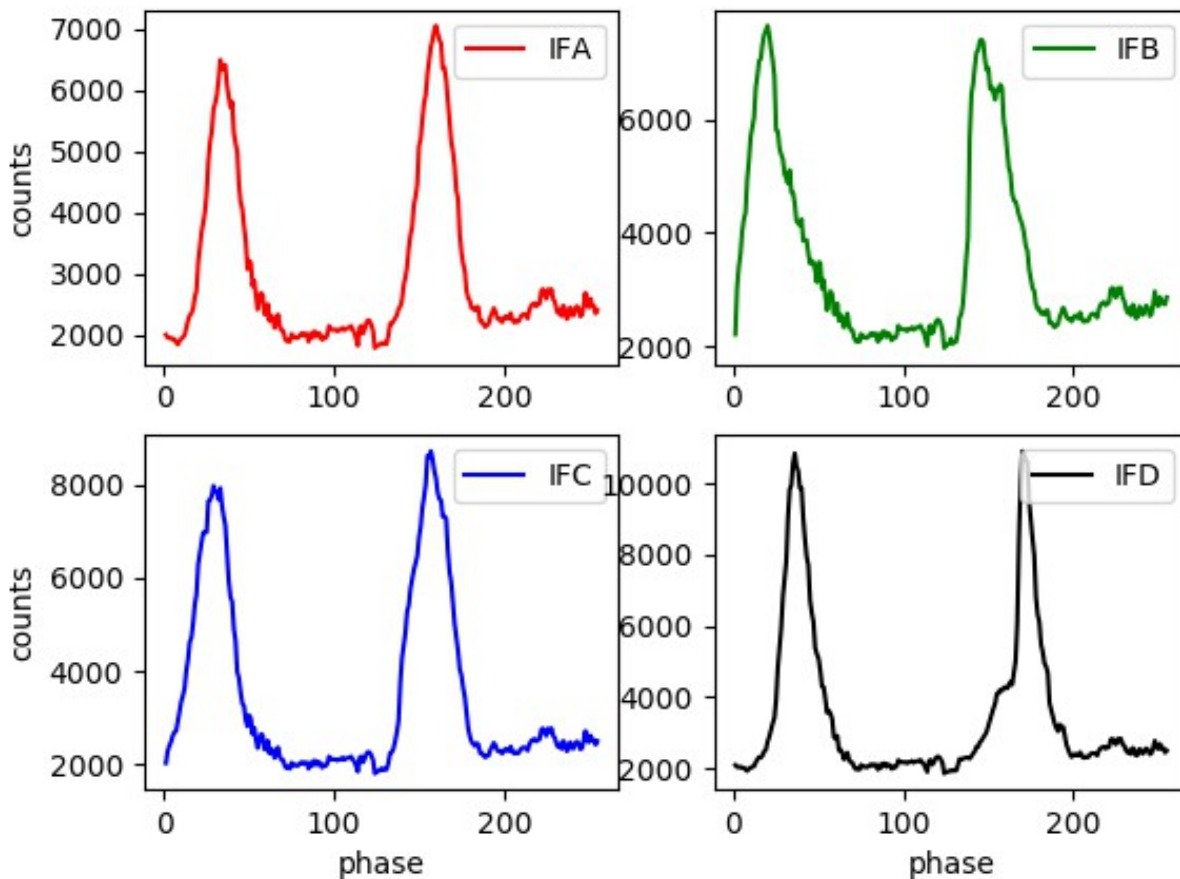
- Connect a synthesizer tuned to 764 MHz to all Ifs or a broad band IF signal (not too strong).
- Load the firmware to test.
- Point all dbbcifa,b,c,d to this input and set AGC to manual, e.g.
 - dbbcifa=1,40,1 # adjusted to about 10000 counts
 - In DDC mode: turn off AGC for BBCs: dbbcgain=all,20,20
- Run the DBBC command: calibration=all
- ... wait

Description at:

https://deki.mpifr-bonn.mpg.de/GMVA/GMVA_HOWTO/DBBC2_calibration



Calibration of the DBBC



...
 252 106 3959 16276 10431
 253 135 5588 17455 10729
 254 161 5276 18712 11039
 255

minM1 00050 ele1 **107** minM2 00050 ele2 **79** minM3 00049 ele3 **92** minM4 00051 ele4 **124**

....				
60	270437	872	261803	16988
61	285347	653	205494	12851
62	289611	395	169170	10302
63	301585	352	144859	7090
64	309365	169	111552	3386
65	317749	102	95884	2313
66	322930	79	79745	1817
67	339064	67	54644	1305
68	332014	57	37490	881
69	338031	55	28940	526
70	324313	54	22799	296
71	320547	52	17611	223
72	310049	51	10504	187
73	276350	51	6440	148
74	260401	51	4751	106
75	251864	51	3334	84
76	204246	51	2061	76
77	169837	51	1407	60
78	149612	51	1155	56
79	97942	51	361	54
80	74886	51	228	53
81	55966	50	130	53
82	46097	51	113	53
83	28929	51	80	53
84	21030	53	69	52
85	7957	55	59	52
86	5530	55	51	52
87	2958	57	51	52
88	2078	61	50	52
89	1368	80	50	52
90	734	79	50	52
91	247	117	50	52
...				



DDC configuration file

c:\DBBC_conf\dbbc_config_file_v107.txt

Example:

```
1 dbbc2_ddc_v107.bit 597.00 8 ← the first number is indication of ADB1|2, in this case ADB1 is on
1 dbbc2_ddc_v107.bit 682.00 8   IFA and ADB2 on IFB, ADB1 in IFC, no Core2 for IFD
1 dbbc2_ddc_v107.bit 853.00 8   If no Core2 is inserted in the first and second column put 0.
1 dbbc2_ddc_v107.bit 938.00 8   The second parameter is the firmware file name to be used.
2 dbbc2_ddc_v107.bit 597.00 8   The third and fourth parameters are frequency and bandwidth respectively.
2 dbbc2_ddc_v107.bit 682.00 8
2 dbbc2_ddc_v107.bit 853.00 8
2 dbbc2_ddc_v107.bit 938.00 8
1 dbbc2_ddc_v107.bit 597.00 8
1 dbbc2_ddc_v107.bit 682.00 8
1 dbbc2_ddc_v107.bit 853.00 8
1 dbbc2_ddc_v107.bit 938.00 8
0 dbbc2_ddc_v107.bit 597.00 8   Each Core2 board supports 4 bbcs so if not present 0 has to be inserted in
0 dbbc2_ddc_v107.bit 682.00 8   four lines
0 dbbc2_ddc_v107.bit 853.00 8
0 dbbc2_ddc_v107.bit 938.00 8
1 fla10g_v2_1.bit COM2 ← if installed set 1st version 1 (with ACE), 2nd version (without ACE 2), otherwise 0, ser. port
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFA
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFB
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFC
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFD
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFE
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFF
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFG
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFH
100 100 100 100 ← phase calibration values
CAT2 1024 ← CAT1|2 and sampling frequency
PROG 0 3 ← jtag programmer: 0=xilinx, 1=digilent; prog freq. 3/6 MHz
```



Test recordings

- Test recordings are good to control the correct sampling (bit statistics), band pass shape, and pcal tones
- The Mark5B comes with a set of programs that allow to check the bit statistics (bstate), do auto- or cross correlations (vlbi2), and extract phase cal (bpcal).
- More power full are the mark5access programs: m5bstate, m5pcal, m5spec, m5timeseries, ...
Available from the EVN TOG wiki pages
https://deki.mpifr-bonn.mpg.de/Working_Groups/EVN_TOG/DBBC/DBBC_Test_Procedures
- jive5ab allows to stream data directly on a local disk, which avoids to record on diskpacks and use disk2file for small tests.



Test recordings

```
oper@eff-mark5c-1:~$ m5spec
```

m5spec ver. 1.3.1 Walter Brisken, Chris Phillips 20120508

A Mark5 spectrometer. Can use VLBA, Mark3/4, and Mark5B formats using the mark5access library.

Usage : m5spec <infile> <dataformat> <nchan> <nint> <outfile> [<offset>]

<infile> is the name of the input file

<dataformat> should be of the form: <FORMAT>-<Mbps>-<nchan>-<nbit>, e.g.:

VLBA1_2-256-8-2

MKIV1_4-128-2-1

Mark5B-512-16-2

VDIF_1000-64-1-2 (here 1000 is payload size in bytes)

<nchan> is the number of channels to make per IF

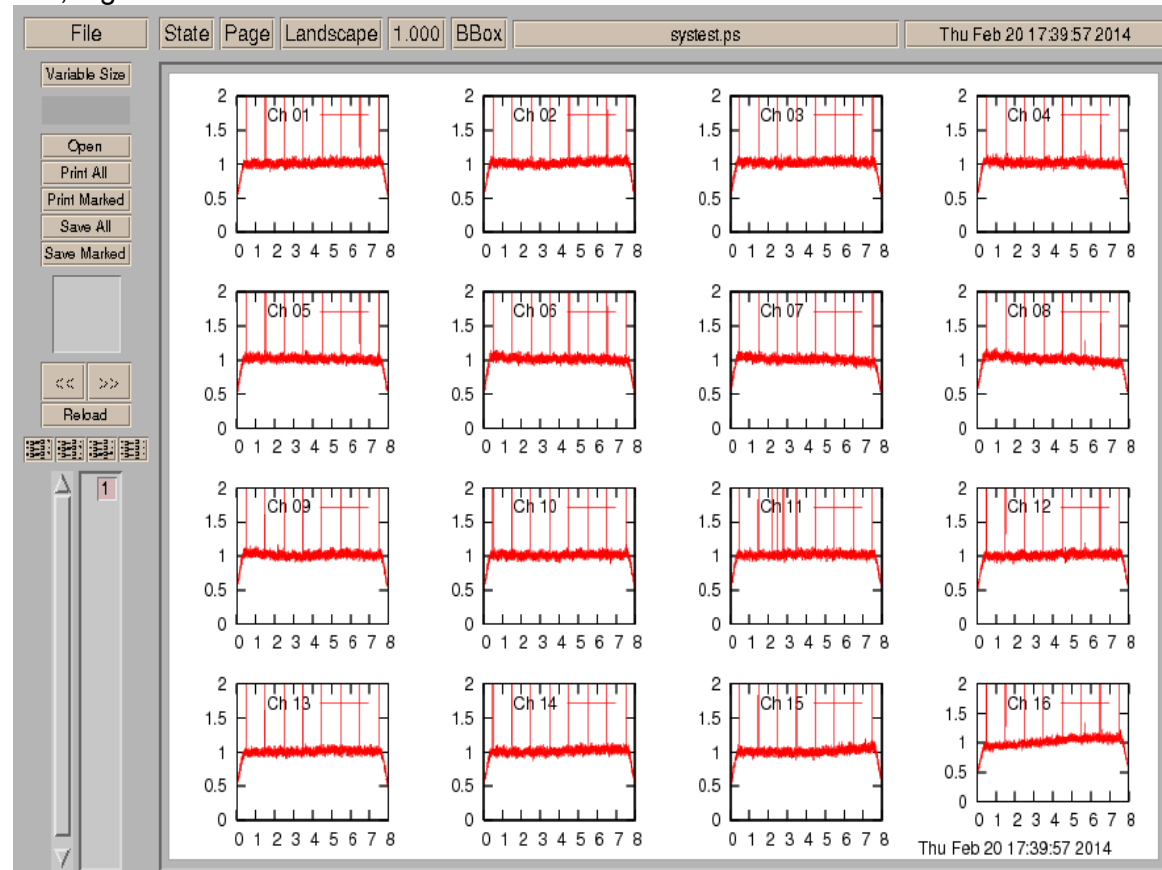
<nint> is the number of FFT frames to spectrometize

<outfile> is the name of the output file

<offset> is number of bytes into file to start decoding

The following options are supported

- dbbc Assume dBBC polarisation order (all Rcp then all Lcp)
- nopol Do not compute cross pol terms
- help This list





Test recordings

> bstate

Usage: bstate <input m5b fname> <# frames>

> bstate n13c1_ef_no0002.m5a 200

Ch	--	-	+	++	-	-	+	++	gfact
0	88032	157895	160426	93647	17.6	32.1	31.6	18.7	1.00
1	93899	151616	154405	100080	18.8	30.9	30.3	20.0	0.95
2	92338	153774	156561	97327	18.5	31.3	30.8	19.5	0.97
3	91497	154665	157139	96699	18.3	31.4	30.9	19.3	0.97
4	84797	161299	163577	90327	17.0	32.7	32.3	18.1	1.03
5	89860	155939	158073	96128	18.0	31.6	31.2	19.2	0.98
6	88426	157547	159995	94032	17.7	32.0	31.5	18.8	1.00
7	85429	160711	162749	91111	17.1	32.5	32.1	18.2	1.02
8	89485	153806	157650	99059	17.9	31.5	30.8	19.8	0.97
9	92445	150796	154915	101844	18.5	31.0	30.2	20.4	0.95
10	89559	153929	157131	99381	17.9	31.4	30.8	19.9	0.97
11	92958	151219	155066	100757	18.6	31.0	30.2	20.2	0.95
12	89607	153163	157750	99480	17.9	31.6	30.6	19.9	0.97
13	84856	158081	162791	94272	17.0	32.6	31.6	18.9	1.01
14	84164	159461	163177	93198	16.8	32.6	31.9	18.6	1.02
15	83381	159953	163898	92768	16.7	32.8	32.0	18.6	1.02



Test recordings

○ > *vlbi2*

vlbi file1 file2 -proctime proctime [-rev <0|1>] [-2bit <0|1>] [-tforce <0|1>]

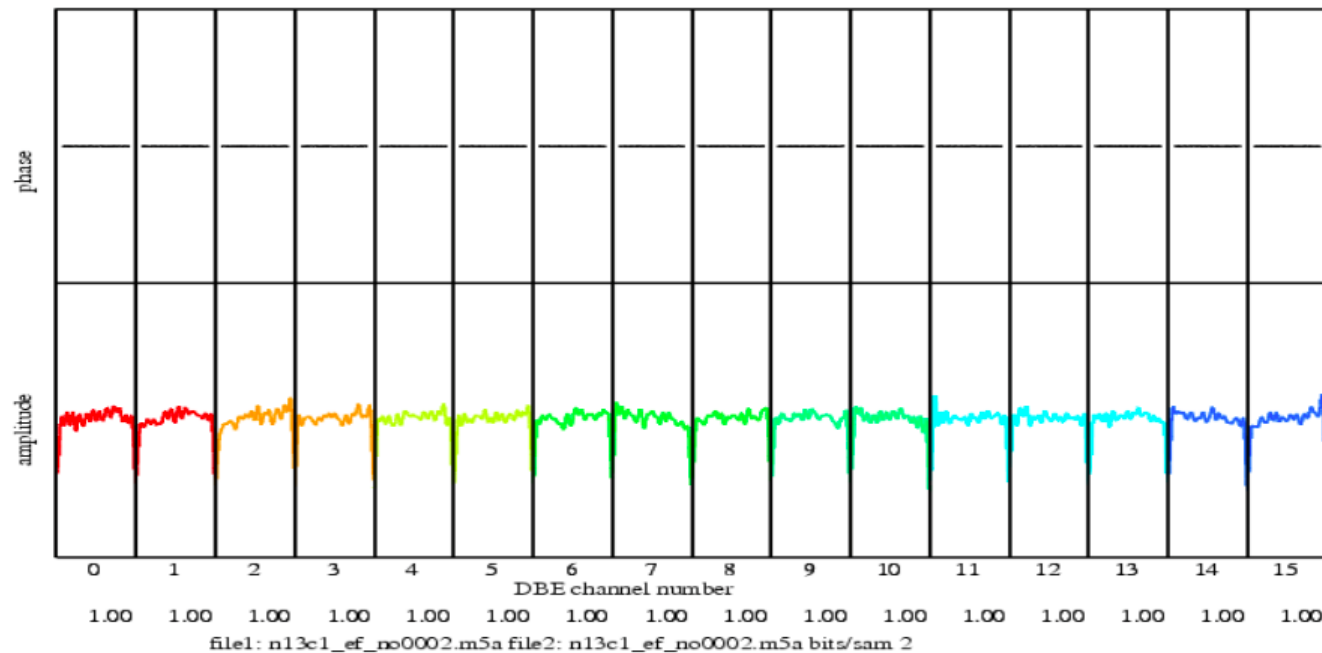
2bit: 1 to enable 2-bit input

rev: 1 to reverse channels in the plot

tforce: 1 to force correlation, ignoring timestamps

> *vlbi2 n13c1_ef_no0002.m5a n13c1_ef_no0002.m5a -2bit 1 # for autocorrelation*

> *gv dd1.pos*





Test recordings

- `> bpcal`

Usage: `bpcal <input m5b fname> <tone freq (KHz)> <# frames>`

`> bpcal n13c1_ef_no0002.m5a 2490 500`

`integration time 0.078 sec`

`ch amp phase(dg)`

`0 1 153.7`

`1 0 -93.5`

`2 1 83.2`

`3 2 -20.0`

`4 1 -54.9`

`5 2 -111.1`

`6 0 -179.6`

`7 1 -152.4`

`8 12 -94.5`

`9 11 -82.5`

`10 11 -69.3`

`11 12 -47.9`

`12 12 24.3`

`13 12 -58.8`

`14 10 -154.2`

`15 9 134.2`



Estimate the best IF level

- IF commands (dbbcifa, or ifa (FS)) allow to specify values for the IF target counts where the AGC should adjusted to.
- With an increasing number of DBBCs the best target IF levels seem to cluster around 35000 to 45000 counts, but it might be worth to test those for your DBBC.
- Best to use with a true receiver with phase-cal on.
- Then change the attenuation in steps of 2.5 dB over the whole range, while checking detector counts, bbc counts and doing some short 10 sec recordings at the Mark5B
- Analyse the recordings using bpcal to measure the Pcal-tone amplitudes.



Estimate the best IF level

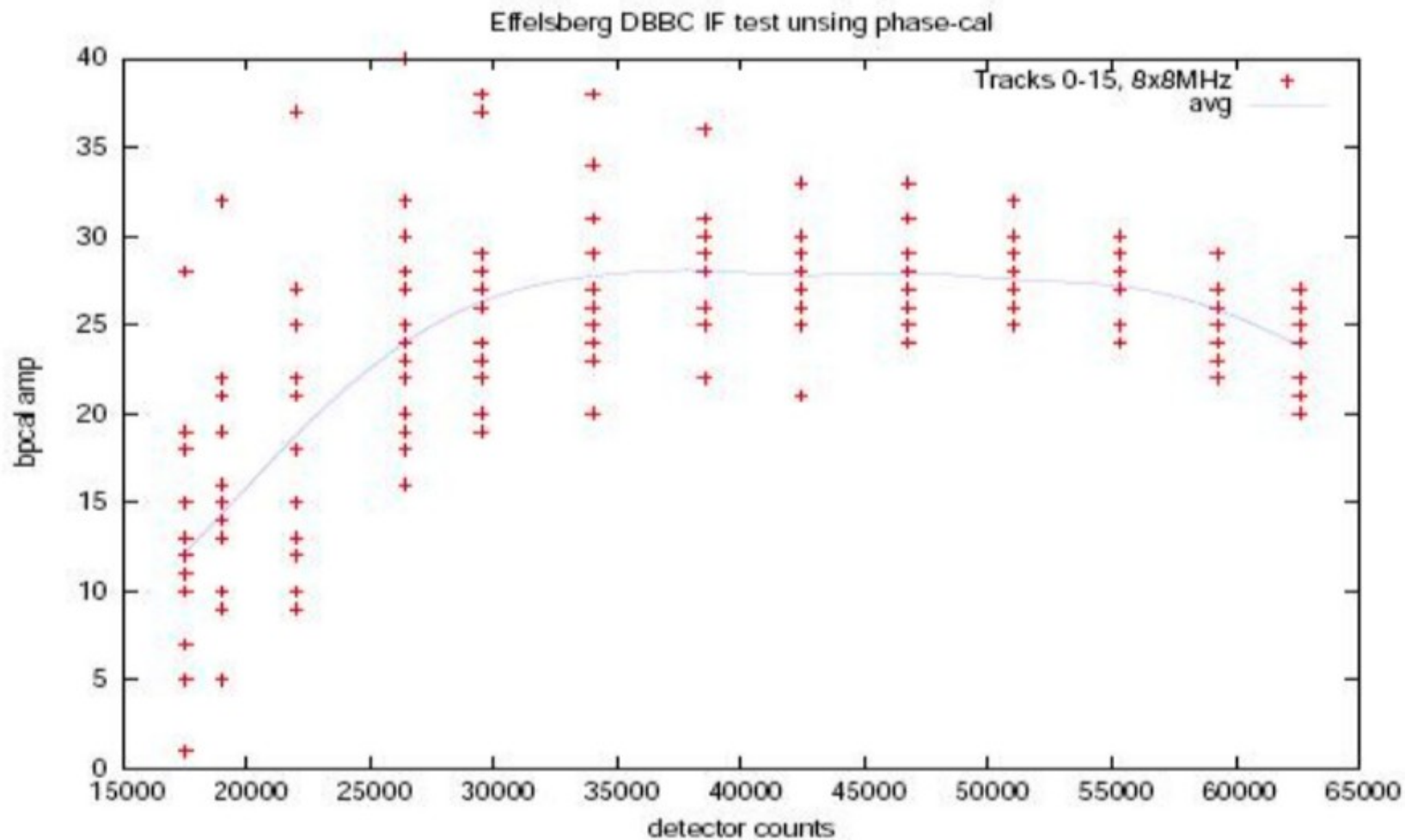


Figure 2: Phase-cal amplitude calculated by bpcal over 0.15 sec against detector counts.



Field System integration

- The DBBC2 is fully integrated into the Field System:
 - It supports both PFB and DDC firmware.
 - Continues calibration in DDC mode.
 - With and without Fila10G.
 - Allows synchronization to internal GPS or NTP on FS-PC.

```
EFLSBERG equipment: Rack=DBBC_DDC/Fil Recorder=FlexBuff
| Select rack          | Select Rec 1 | Select Rec 2 | Start |
| 1=none              | 1=none       | * 1=none     | * 1   |
| 2=Mark3A            | 2=unused     | 2=unused     | 2     |
| 3=VLBA              | 3=Mark3A     | 3=Mark3A     |       |
| 4=VLBA4             | 4=VLBA       | 4=VLBA       |       |
| 5=VLBA4/8          | 5=VLBA4     | 5=VLBA4     |       |
| 6=VLBA4/8          | 6=Mark4      | 6=Mark4      |       |
| 7=Mark4             | 7=S2         | 7=S2         |       |
| 8=VLBA4            | 8=K4-1       |               |       |
| 9=K4-1             | 9=K4-2       |               |       |
| 10=K4-2            | 10=Mark5A    |               |       |
| 11=K4-1/K3         | 11=Mk5APigW  |               |       |
| 12=K4-2/K3         | 12=Mark5P    |               |       |
| 13=K4-1/M4         | 13=K5        |               |       |
| 14=K4-2/M4         | 14=Mark5B    |               |       |
| 15=LBA              | 15=Mark5C    |               |       |
| 16=Mark5            | *16=FlexBuff |               |       |
| 17=VLBA5           |               |               |       |
| 18=DBBC_DDC         |               |               |       |
| *19=DBBC_DDC/Fila10g |               |               |       |
| 20=DBBC_PFB         |               |               |       |
| 21=DBBC_PFB/Fila10g |               |               |       |
| 22=VLBA4           |               |               |       |
| 23=CDAS             |               |               |       |
| Press <ret> or type 0 for no change. Else <rack><rec1><rec2><start>
| CAUTION! Be sure the schedule works with your choices!
```



Field System integration

- Notes on DBBC2 integration are available in `/usr2/fs/misc/dbbc.txt`
- There are the typical control-files that need to be adapted for a new backend and one special for the DBBC IP address:
 - *dbbad.ctl* hold the DBBC IP address
 - *equip.ctl* for the FS
 - *skedf.ctl* for DRUDG
 - Some more in `point.prc`, `station.prc`, and `.Xresources`
- Once this is done the FS should be ready to DRUDG and observe DBBC schedules.



Field System integration

```
define proc_library 00000000000x
" EUR135 EFLSBERG Ef
" drudg version 2015Jan29 compiled under FS 9.11.07
"< DBBC rack >< Mark5B recorder 1>
enddef
define exper_initi 00000000000x
proc_library
sched_initi
logsw_jv
mk5=DTS_id?
mk5=OS_rev?
mk5=SS_rev?
mk5=status?
enddef
define setupsx 00000000000x
pcalon
tpicd=stop
mk5b_mode=ext,0x55555555,,8.000
mk5b_mode
form=geo
form
dbbcsx4
ifdsx
cont_cal=on,4
bbc_gain=all,agc,12000
tpicd=no,200
bank_check
tpicd
enddef
```

```
define dbbcsx4 00000000000x
bbc01=100.99,a,4.00
bbc02=110.99,a,4.00
bbc03=140.99,a,4.00
bbc04=200.99,a,4.00
bbc05=310.99,b,4.00
bbc06=390.99,b,4.00
bbc07=440.99,b,4.00
bbc08=460.99,b,4.00
bbc09=112.99,c,4.00
bbc10=127.99,c,4.00
bbc11=137.99,c,4.00
bbc12=167.99,c,4.00
bbc13=187.99,d,4.00
bbc14=192.99,d,4.00
enddef
define ifdsx 00000000000x
ifa=4,agc,2,38000
ifb=4,agc,2,38000
ifc=2,agc,2,38000
ifd=2,agc,2,38000
lo=loa,8110.00,usb,rcp,1
lo=lob,8110.00,usb,rcp,1
lo=loc,2100.00,usb,rcp,1
lo=lod,2100.00,usb,rcp,1
enddef
```

Field System integration

Applications Places Tue Apr 30, 9:03 AM VLBI Operator

```
Field System Log
08:51:03&bread/if=bbc15,bbc15
08:51:03&bread/if=bbc16,bbc16
08:51:03&bread/if=pfb.if=core1\,pfb1
08:51:03&bread/if=pfb.if=core2\,pfb2
08:51:03&bread/if=pfb.if=core3\,pfb3
08:51:03&bread/if=pfb.if=core4\,pfb4
08:51:03/bbc01/ 866.490000.a. 8. 1.agc.136.133.11955.11963.11385.11393
08:51:03/bbc02/ 882.490000.a. 8. 1.agc.127.131.11812.11908.11241.11328
08:51:03/bbc03/ 898.490000.a. 8. 1.agc.127.124.11917.11830.11317.11256
08:51:03/bbc04/ 914.490000.a. 8. 1.agc.133.131.12130.12121.11525.11520
08:51:03/bbc09/ 866.490000.c. 8. 1.agc.219.219.10428.10938. 9932.10411
08:51:03/bbc10/ 882.490000.c. 8. 1.agc.219.219.11029.10552.10508.10059
08:51:03/bbc11/ 898.490000.c. 8. 1.agc.218.219.11835.10946.11274.10431
08:51:03/bbc12/ 914.490000.c. 8. 1.agc.219.217.10620.11806.10099.11233
08:51:15:caltsys
08:51:15&caltsys/onsource
08:51:15&caltsys/if=cont_cal.tpiced=tsys.caltsys_man
08:51:15&caltsys/if=cont_cal..ifagc
08:51:15&caltsys/if=cont_cal..if=ddc\,bbc_gain=all\\\.agc
08:51:15#antcn#Antenna TRACKING
08:51:15#antcn# RFcentre wanted: 4850 Antenna: 4850 synth1,2= 613.000000 0.000000
08:51:15/onsource/TRACKING
08:51:27/tpi/11.11399.2.1u.11377.2.21.11337.0.2u.11246.8.31.11260.2.3u.11331.2.41.11537.2
08:51:27/tpi/4u.11536.5.ia.1838.33
08:51:27/tpi/91.11316.2.9u.11220.5.al.11290.0.au.11320.8.bl.11233.2.bu.11298.0.cl.11264.2
08:51:27/tpi/cu.11267.5.ic.1787.60
08:51:27/tpical/11.11976.0.1u.11960.8.21.11921.2.2u.11820.0.31.11842.8.3u.11914.2.41.12124.0
08:51:27/tpical/4u.12129.0
08:51:27/tpical/91.11888.8.9u.11788.2.al.11855.5.au.11886.2.bl.11793.2.bu.11867.2.cl.11837.2
08:51:27/tpical/cu.11835.8
08:51:27/caltemp/11.1.836.1u.1.840.21.1.841.2u.1.837.31.1.838.3u.1.846.41.1.854.4u.1.890
08:51:27/caltemp/91.1.817.9u.1.812.al.1.806.au.1.797.bl.1.793.bu.1.801.cl.1.817.cu.1.833
08:51:27/tsys/11.36.3.1u.35.9.21.35.7.2u.36.0.31.35.5.3u.35.9.41.36.4.4u.36.8
08:51:27/tsys/91.35.9.9u.35.8.al.36.0.au.36.0.bl.36.0.bu.35.7.cl.35.7.cu.36.3
```

```
VLBI-Server (Wichtig nicht schliessen! r wiederholt den letzten Befehl)
input do nothing

Mark6-VLBI-Monitor
r V0.997
alized value $mk6state in string eq at /usr2/oper/bin/zl
line 537. : laeuft | OK
c zu 1pps : | OK
t korrekt : | OK
det Daten : e-VLBI stoppedessenen! | OK
-----
Mark6-System
: laeuft | OK
-----
: 0 %
e-VLBI
ler:
el: | OK
IES: | ULO OK
sr2/log/em135bef.log

30.Apr. 2019 Day 120 09:03:40

tit: q (15 sec Verzoeigerung) Feb 2016 by AK/DG/UB
```

System Temperatur

tsys	0.0	(IFA)	(IFB)
bbc	0.0	(IFC)	(IFD)
01	866.49	35.9	36.3
02	882.49	36.0	35.7
03	898.49	35.9	35.5
04	914.49	36.8	36.4
05			
06			
07			
08			
09	866.49	35.8	35.9
10	882.49	36.0	36.0
11	898.49	35.7	36.0
12	914.49	36.3	35.7
13			
14			
15			
16			

System Status

```
EFLSBERG 2019.120.09:03:48 UT TEMP 9.5C 3c48 TRACKING
MODE RATE 09:06:11 NEXT HUMID 83.17% RA 01h37m41.3s
SCHED=none LOG=station PRES 984.8mb DEC 33d09m (2000)
TSYS: IFA IFB IFC IFD CABLE 0.000000s AZ 125.8 EL 65.5
0 0 0 0
```

NO CHECK: rx

ERRORS

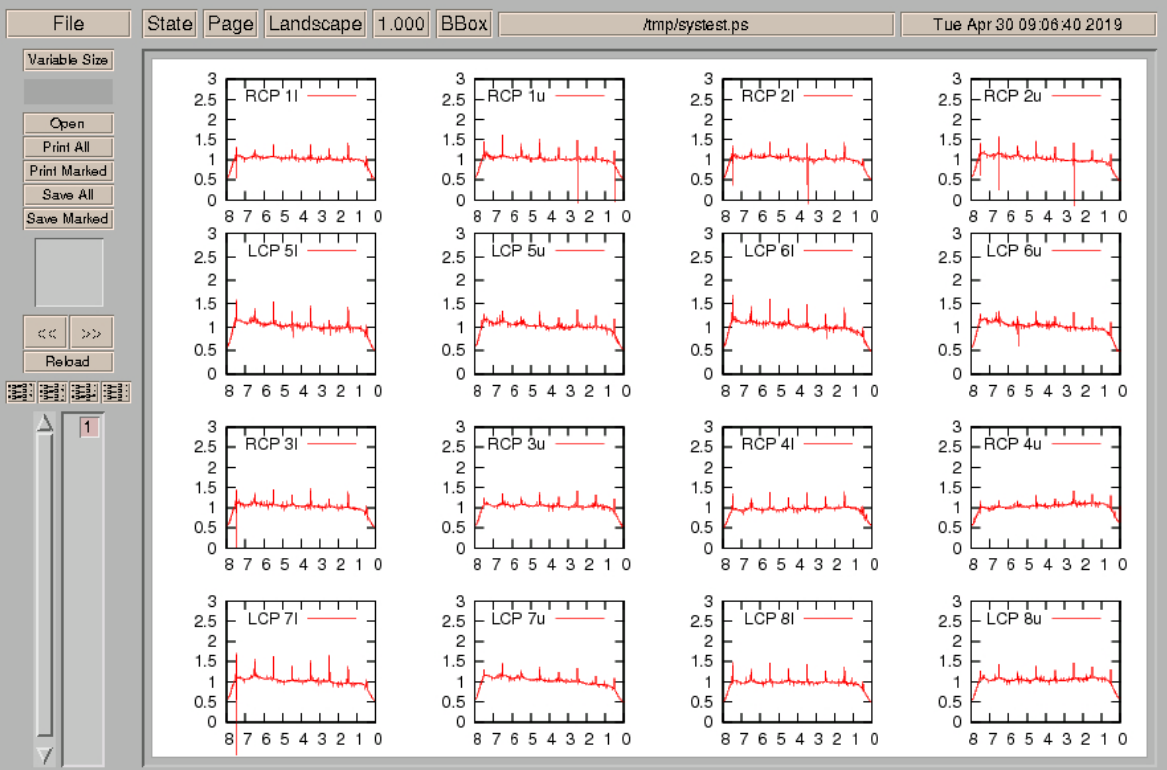
```
Operator Input
>proc=n13clef
>setup01
>3c48
>iread
>bread
>caltsys
>
```

DBBC

Field System integration

Field System Log

gv: /tmp/systest.ps (on Mark6-4040)



Warning: Cannot convert string "-efont-biwidth-medium-r-normal--16-*-*-*-*-*iso10646-1,-gnu-unifont-medium-r-normal--16-*-*-*-*-*iso10646-1,-adobe-helvetica-medium-r-normal--14-*-*-*-*-*,-jis-fixed-medium-r-*--16-*-*-*-*-*jisx0208.1983-0,-*-*-*medium-r-*--16-*-*-*-*-*" to type FontSet

BI-Server (Wichtig nicht schliessen! r wiederholt den letzten Befehl)

```

> send >>SV NONE 3c48 1b37m41 3c 33d09'35" 4850 00560mm ulbi 0 0 2000NON to bed
Mark6-VLBI-Monitor
r V0.997
alized value $mk6state in string eq at /usr2/oper/bin/zl
line 537. : laeuft | OK
c zu 1pps : | OK
t korrekt : | OK
det Daten : e-VLBI stoppedessenen! | OK
-----
Mark6-System
: laeuft | OK
0 %
e-VLBI
ler:
el: | OK
IES: | ULO OK
sr2/log/em135bef.log
30.Apr. 2019 Day 120 09:06:52
it: q (15 sec Verzoeigerung) Feb 2016 by AK/DG/UB
    
```

System Temperatur

TSys	0.0 (IFA)	(IFB)	
BBC	freq	ts-U	ts-L
01	866.49	35.9	36.3
02	882.49	36.0	35.7
03	898.49	35.9	35.5
04	914.49	36.8	36.4
05			
06			
07			
08			
09	866.49	35.8	35.9
10	882.49	36.0	36.0
11	898.49	35.7	36.0
12	914.49	36.3	35.7
13			
14			
15			
16			

System Status

```

EFLSBERG 2019.120.09:06:54 UT TEMP 9.5C 3c48 TRACKING
MODE RATE 09:11:38 NEXT HUMID 77.57% RA 01h37m41.3s
SCHED=none LOG=station PRES 984.7mb DEC 33d09m (2000)
TSYS: IFA IFB IFC IFD CABLE 0.000000s AZ 127.0 EL 65.9
0 0 0 0
NO CHECK: rX
    
```

ERRORS

Operator Input

```

>caltsys
>mk5-record=test_ef_no0430
>mk5-record=on:test_ef_no0430
>mk5-record?
>mk5-record?
>mk5-record=off
>checkmk5
>pcalon
>mk5-record=on:test_ef_no0431
>mk5-record=off
>
    
```

Field System integration

Field System Log

```
sample rate = 16000000 Hz
offset = 0
framebytes = 8032 bytes
datasize = 8000 bytes
sample granularity = 1
frame granularity = 1
gframens = 125000
payload offset = 32
read position = 0
data window size = 1048576 bytes
```

Ch	--	-	+	++	--	-	+	++	gfact
0	138368	262632	262243	136757	17.3	32.8	32.8	17.1	1.04
1	137356	263934	262360	136350	17.2	33.0	32.8	17.0	1.04
2	140120	261046	260263	138571	17.5	32.6	32.5	17.3	1.03
3	152449	249598	268300	129653	19.1	31.2	33.5	16.2	1.02
4	138858	263584	261868	135690	17.4	32.9	32.7	17.0	1.04
5	138883	263806	261438	135873	17.4	33.0	32.7	17.0	1.04
6	138185	263866	261590	136359	17.3	33.0	32.7	17.0	1.04
7	139228	263236	256358	141178	17.4	32.9	32.0	17.6	1.03
8	135818	262091	263365	138726	17.0	32.8	32.9	17.3	1.04
9	136270	261450	263638	138642	17.0	32.7	33.0	17.3	1.04
10	135398	262259	262153	140190	16.9	32.8	32.8	17.5	1.04
11	104176	293127	250359	152338	13.0	36.6	31.3	19.0	1.09
12	135139	261104	264012	139745	16.9	32.6	33.0	17.5	1.04
13	135031	261317	263550	140102	16.9	32.7	32.9	17.5	1.04
14	135647	260682	263579	140092	17.0	32.6	32.9	17.5	1.04
15	119476	277567	263587	139370	14.9	34.7	32.9	17.4	1.08

800000 / 800000 samples unpacked
8192000 / 8192000 samples unpacked

Warning: Missing charsets in String to FontSet conversion
Warning: Cannot convert string "-efont-biwidth-medium-r-normal--16-*-*-*-*--iso10646-1,-gnu-unifont-medium-r-normal--16-*-*-*-*--iso10646-1,-adobe-helvetica-medium-r-normal--14-*-*-*-*-*,-jis-fixed-medium-r-*--16-*-*-*-*--jisx0208.1983-0,-*-*-*-*--medium-r-*--16-*-*-*-*-*" to type FontSet

System Status

```
EFLSBERG 2019.120.09:05:59 UT TEMP 9.6C 3c48 TRACKING
MODE RATE 09:10:30 NEXT HUMID 80.15% RA 01h37m41.3s
SCHED=none LOG=station PRES 984.7mb DEC 33d09m (2000)
TSYS: IFA IFB IFC IFD CABLE 0.000000s AZ 126.7 EL 65.8
0 0 0 0
NO CHECK: rx
```

ERRORS

VLBI-Server (Wichtig nicht schliessen! r wiederholt den letzten Befehl)

```
Mark6-VLBI-Monitor
r V0.997
alized value $mk6state in string eq at /usr2/oper/bin/zl
line 537. : laeuft | OK
c zu 1pps : | OK
t korrekt : | OK
det Daten : e-VLBI stoppedessenene! | OK
Mark6-System
: laeuft | OK
0 %
e-VLBI
ler:
el: | OK
IES: | ULO OK
sr2/log/em135bef.log
30.Apr. 2019 Day 120 09:05:54
it: q (15 sec Verzoeigerung) Feb 2016 by AK/DG/UB
```

System Temperatur

TSys	IFA	IFB	
01	866.49	35.9	36.3
02	882.49	36.0	35.7
03	898.49	35.9	35.5
04	914.49	36.8	36.4
05			
06			
07			
08			
09	866.49	35.8	35.9
10	882.49	36.0	36.0
11	898.49	35.7	36.0
12	914.49	36.3	35.7
13			
14			
15			
16			

Operator Input

```
>setup01
>3c48
>iread
>bread
>caltsys
>mk5-record=test_ef_no0430
>mk5-record=on:test_ef_no0430
>mk5-record?
>mk5-record?
>mk5-record=off
>
```




DBBC2 resources

- DBBC2 software, firmware and documents:
<http://www.hat-lab.com> (until 2018)
<https://www.hat-lab.cloud>
- DBBC2 installation, testing, and operational notes:
https://deki.mpifr-bonn.mpg.de/Working_Groups/EVN_TOG
<https://deki.mpifr-bonn.mpg.de/GMVA>